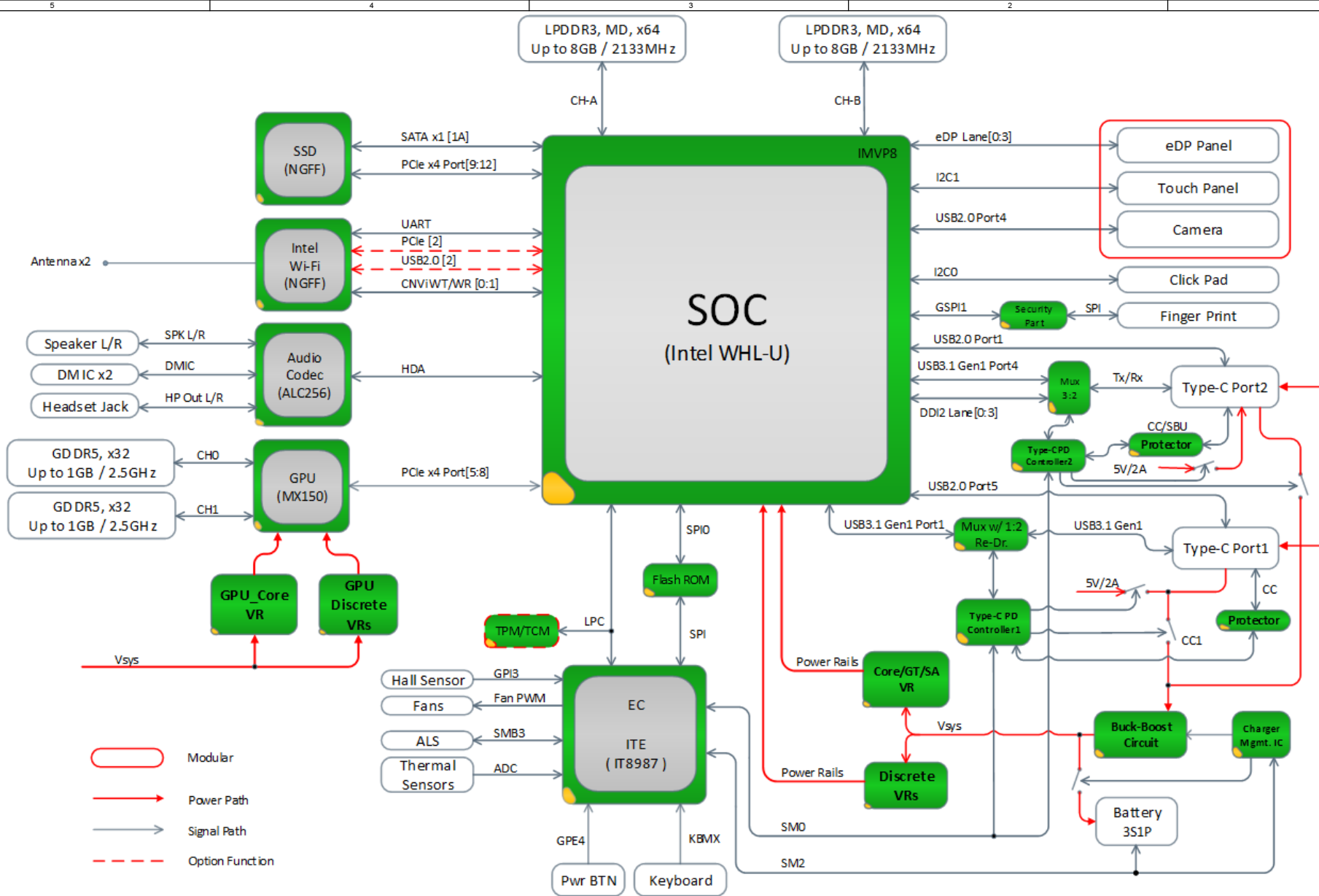
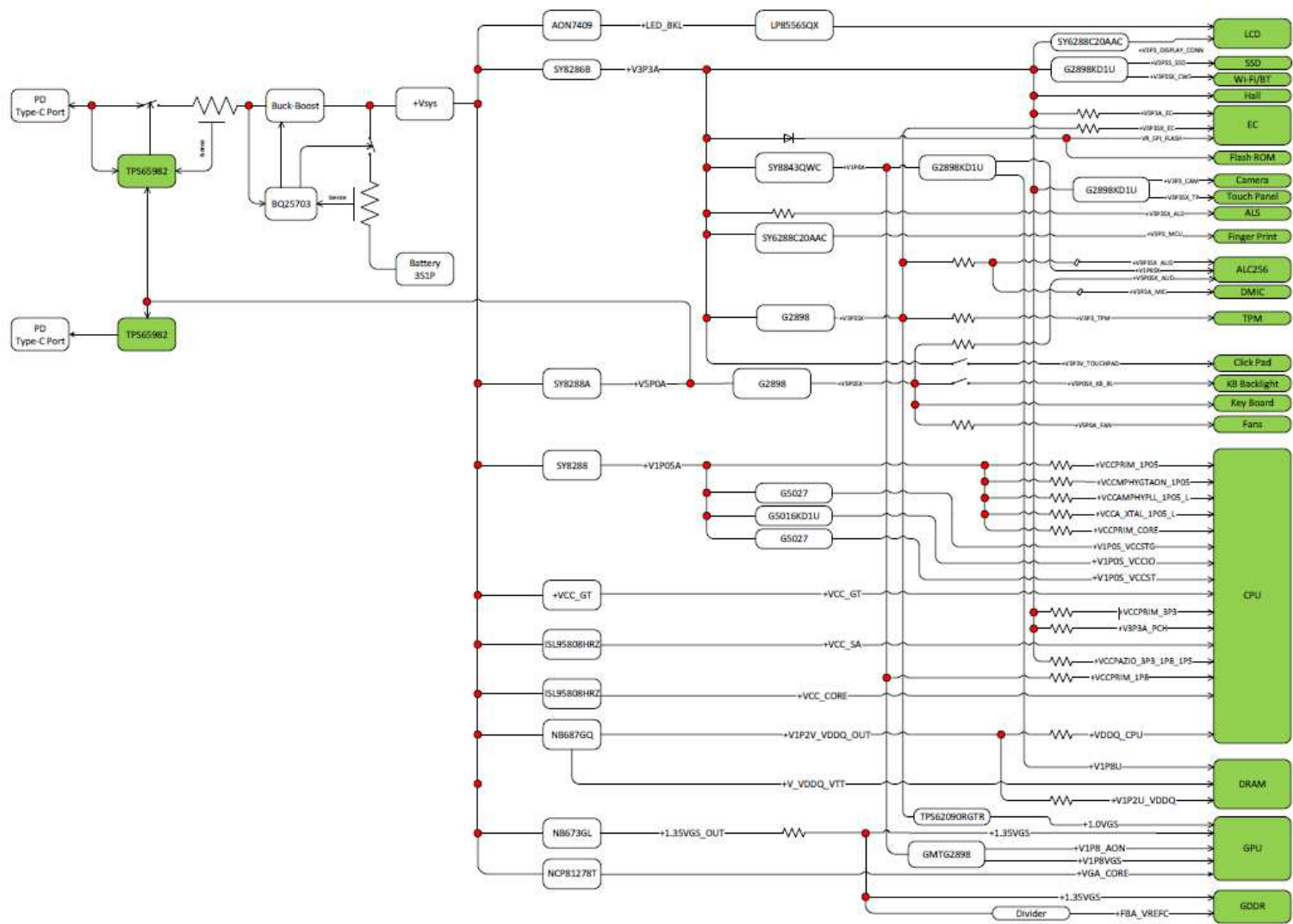


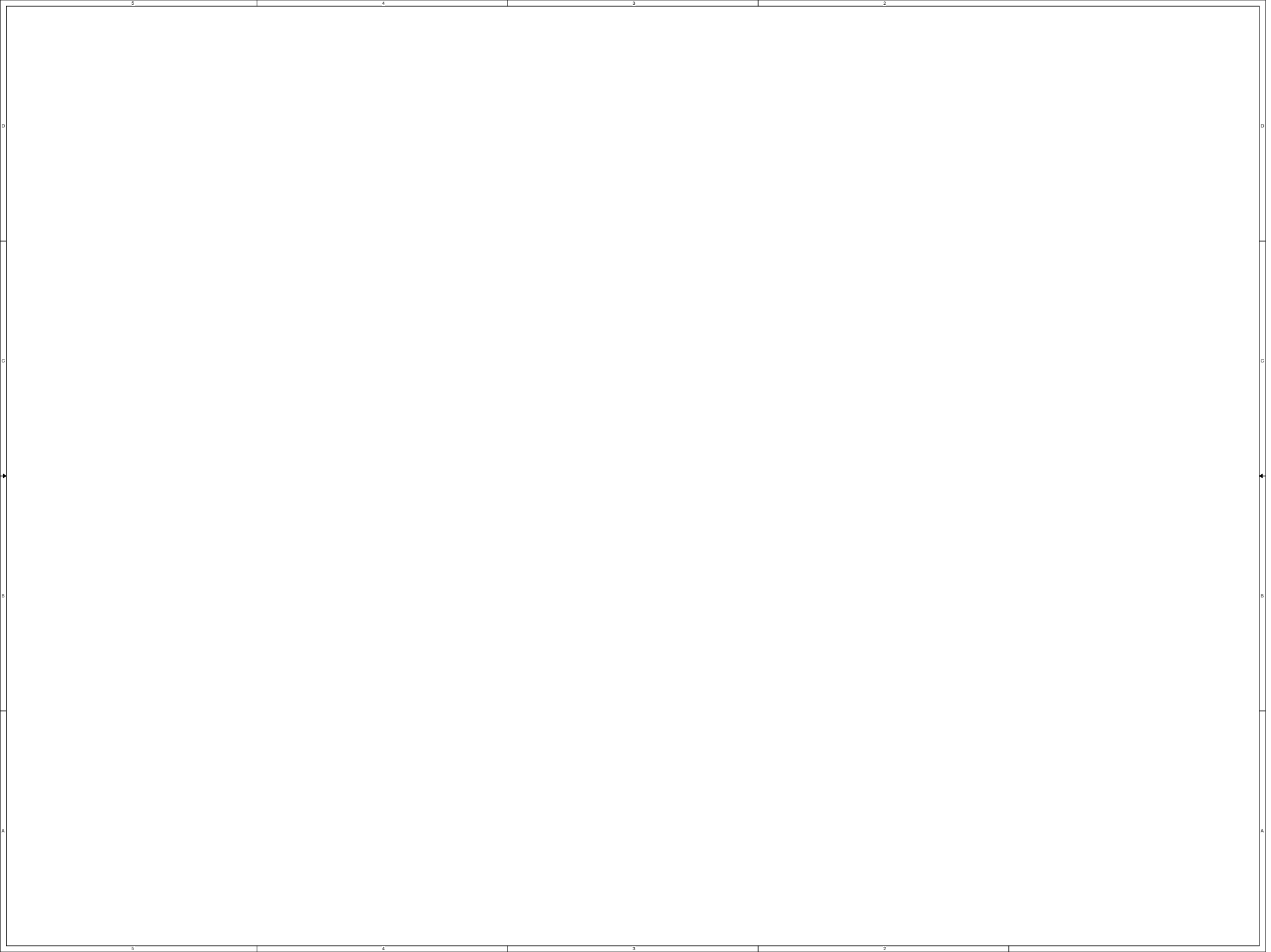
Schematics Page Index (Title / Revision / Change Date)

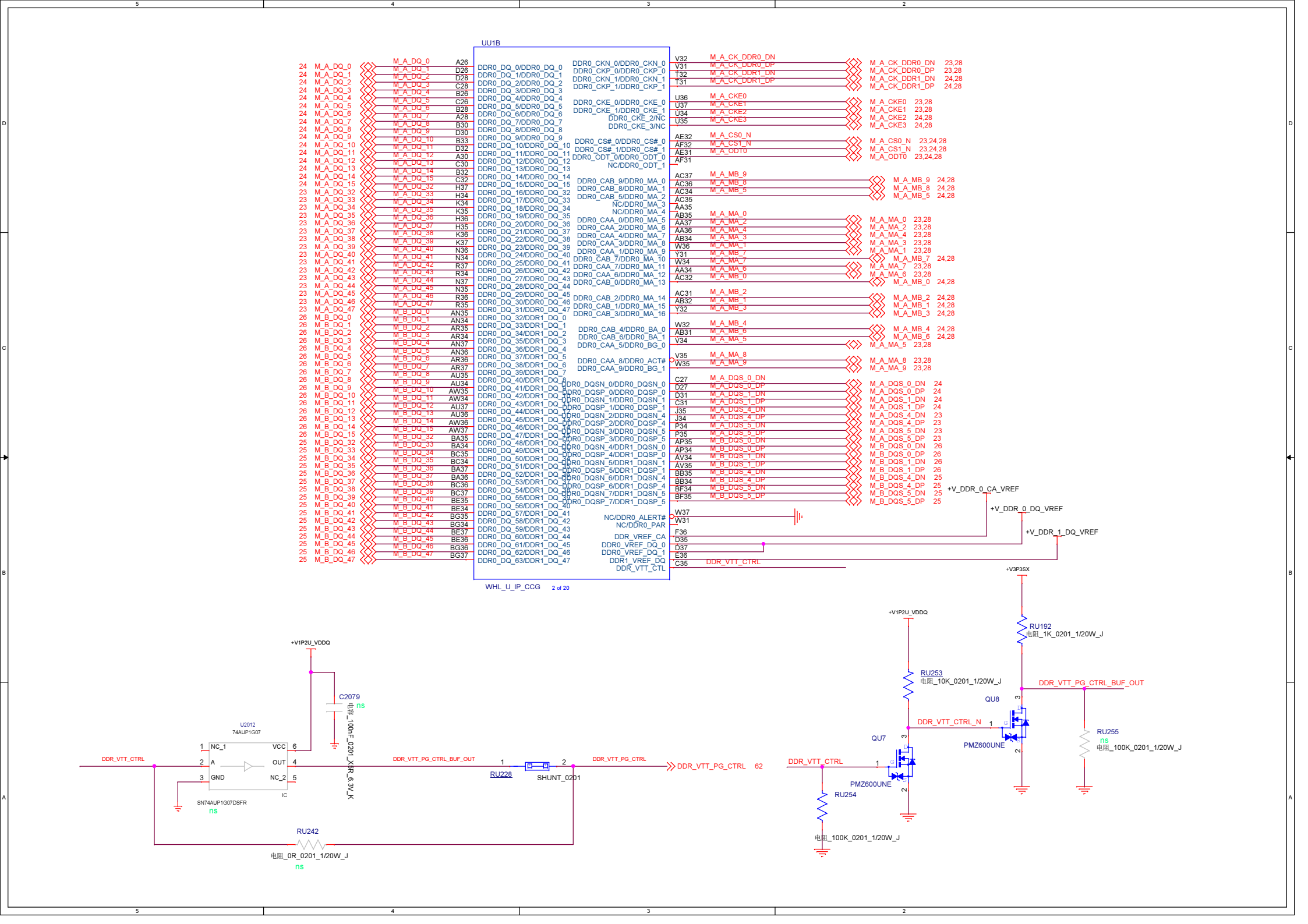
Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page		
01	Index	1.0		35	EDP & CAM&TP	1.0	
02	Block Diagram	1.0		36	BLANK	1.0	
03	Power Map	1.0		37	Codec	1.0	
04	I2C Table	1.0		38	M.2 SSD	1.0	
05	Blank	1.0		39	WLAN WIFI BT MODULE	1.0	
06	WHL-U42 (CHA)	1.0		40	BLANK	1.0	
07	WHL-U42 (CHB)	1.0		41	KB CON & Backlight	1.0	
08	WHL-U42 (DISPLAY)	1.0		42	EC(IT8987E)	1.0	
09	WHL-U42 (SPI/LPC/ESPI/XDP)	1.0		43	BUTTON/FAN/LED/Hall	1.0	
10	WHL-U42 (CNV1/EMMC/CLK)	1.0		44	TouchPad	1.0	
11	WHL-U42 (HDA/SD/I2C/GPIO)	1.0		45	MCP&Finger Print conn	1.0	
12	WHL-U42 (USB/PCIE)	1.0		46	RSMRST OFF	1.0	
13	WHL-U42 (PMU)	1.0		47	N17S PCIE/ CLK/ GPIO	1.0	
14	WHL-U42 (VCORE/GT)	1.0		48	N17S DISPLAY/ STRAP/ JTAG	1.0	
15	WHL-U42 (PCH)	1.0		49	N17S MEM Power	1.0	
16	WHL-U42 (VCC/VDDQ)	1.0		50	N17S +VGA CORE, GND	1.0	
17	WHL-U42 (VSS)	1.0		51	N17S MEM Interface	1.0	
18	WHL-U42 (CFG)	1.0		52	N17S GDDR5	1.0	
19	WHL-U42 (DECOUPLING1)	1.0		53	N17S MISC	1.0	
20	WHL-U42 (DECOUPLING2)	1.0		54	sensor	1.0	
21	WHL-U42 (DECOUPLING3)	1.0		55	TPM	1.0	
22	WHL-U42 (DECOUPLING4)	1.0		56	POWER DCIN & BATTERY CHARGER	1.0	
23	LPDDR3 CH-A 1	1.0		57	POWER DELIVERY 3.3V	1.0	
24	LPDDR3 CH-A 2	1.0		58	POWER DELIVERY 5V	1.0	
25	LPDDR3 CH-B 1	1.0		59	POWER DELIVERY 1.8V	1.0	
26	LPDDR3 CH-B 2	1.0		60	POWER DELIVERY 1.05V	1.0	
27	LPDDR3 (DECAPS)	1.0		61	POWER DELIVERY-IMVP1	1.0	
28	LPDDR3 TERMINATIONS	1.0		62	POWER DELIVERY 1.2V	1.0	
29	SYSTEM FLASH	1.0		63	POWER DELIVERY 1.35VGS	1.0	
30	TYPE1-C PD & MUX	1.0		64	POWER DELIVERY 1.0VGS&1.8VGS	1.0	
31	TYPE1-C CONN	1.0		65	POWER DELIVERY-GPU Core	1.0	
32	TYPE2-C PD & MUX	1.0		66	POWER DELIVERY Load switch	1.0	
33	TYPE2-C CONN	1.0		67	LED BACKLIGHT	1.0	
34	BLANK	1.0		68	Debug Conn	1.0	
				69	Hole & Mark	1.0	
				70	Changelist	1.0	



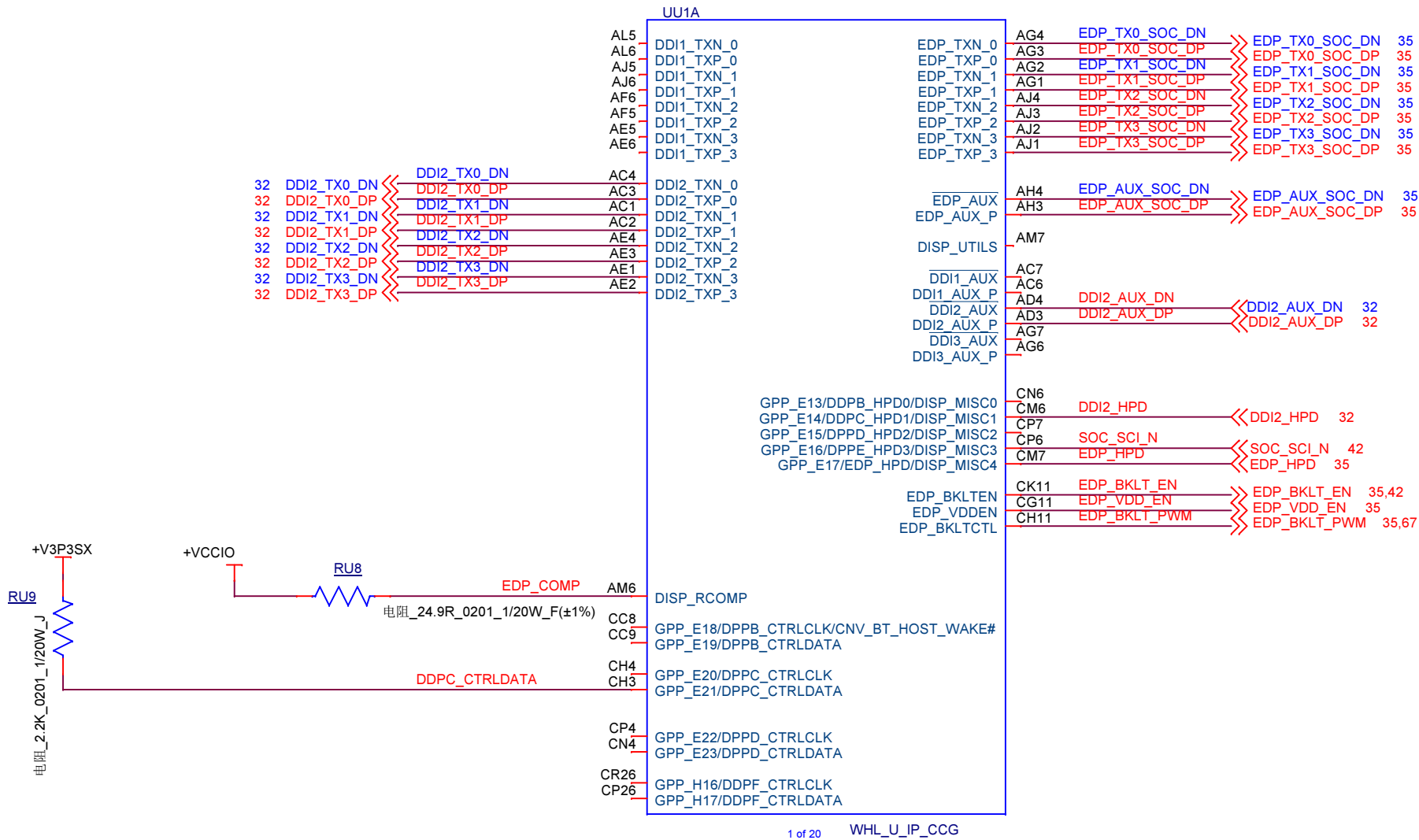


I2C Allcation Mapping						
EC	Device1		Device2		Device3	
SMCLK0 SMDAT0	Type-C1(PD)	address:TBD	Type-C2(DP)	address:TBD	ALS	address:0x29H
SMCLK1 SMDAT1	Battery	address:TBD	x	x	x	x
SMCLK2 SMDAT2	Charger	address:TBD	DGPU Internal Thermal Sensor	address:TBD	Touch panel Back Light	address:TBD
SMCLK3 SMDAT3	Debug	address:TBD	x	x	x	x
SOC	Device1		Device2		Device3	
I2C_CLK0 I2C_DAT0	TOUCHPAD	address:TBD	X	X	X	X
I2C_CLK1 I2C_DAT1	TOUCHPAENL	address:TBD	X	X	X	X
I2C_CLK2 I2C_DAT2	X	X	X	X	X	X
I2C_CLK3 I2C_DAT3	X	X	X	X	X	X
I2C_CLK4 I2C_DAT4	X	X	X	X	X	X
I2C_CLK4B I2C_DAT4B	X	X	X	X	X	X
ISH_I2C_CLK0 ISH_I2C_DAT0	X	X	X	X	X	X
ISH_I2C_CLK1 ISH_I2C_DAT1	X	X	X	X	X	X
ISH_I2C_CLK2 ISH_I2C_DAT2	X	X	X	X	X	X



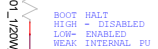


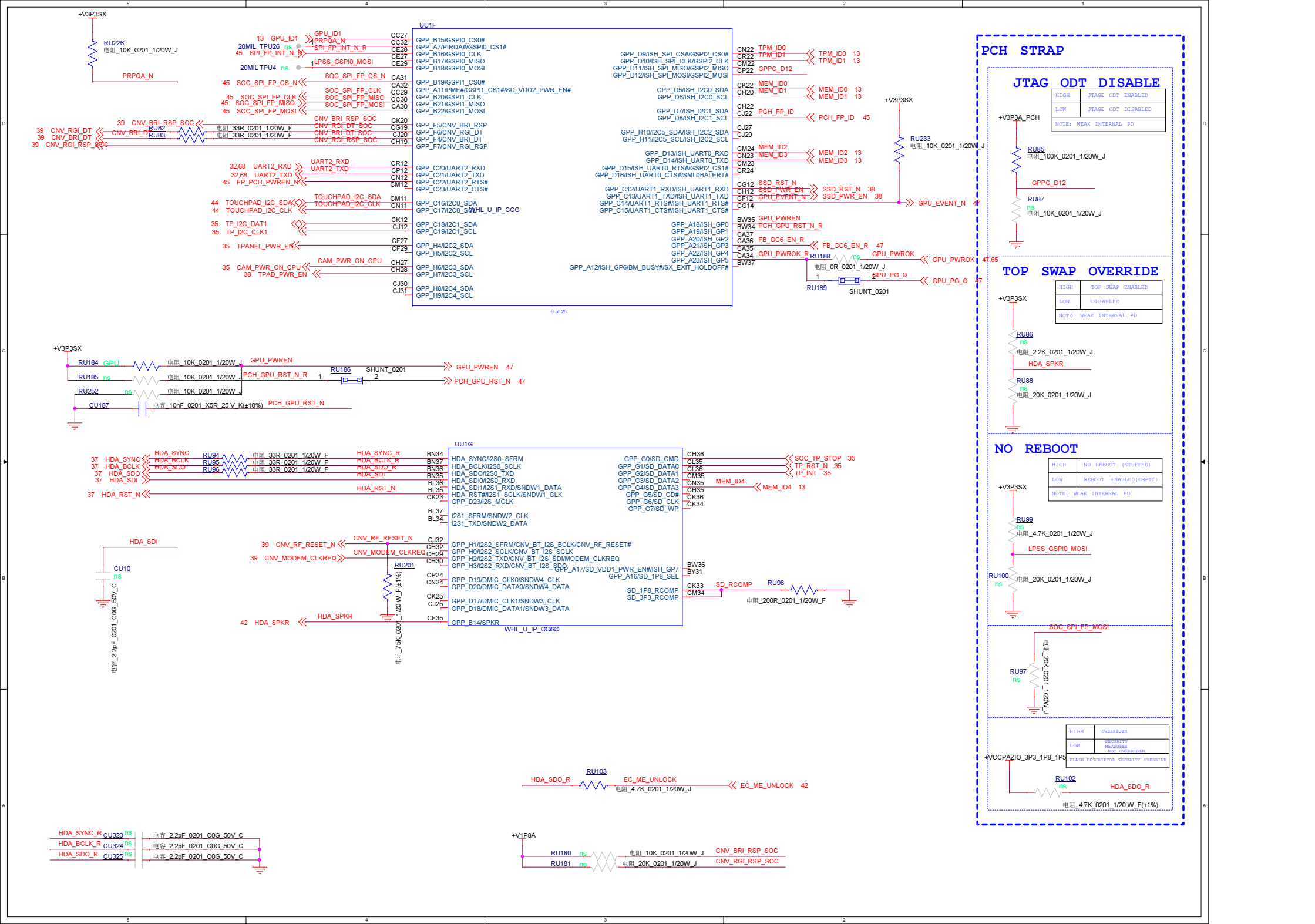


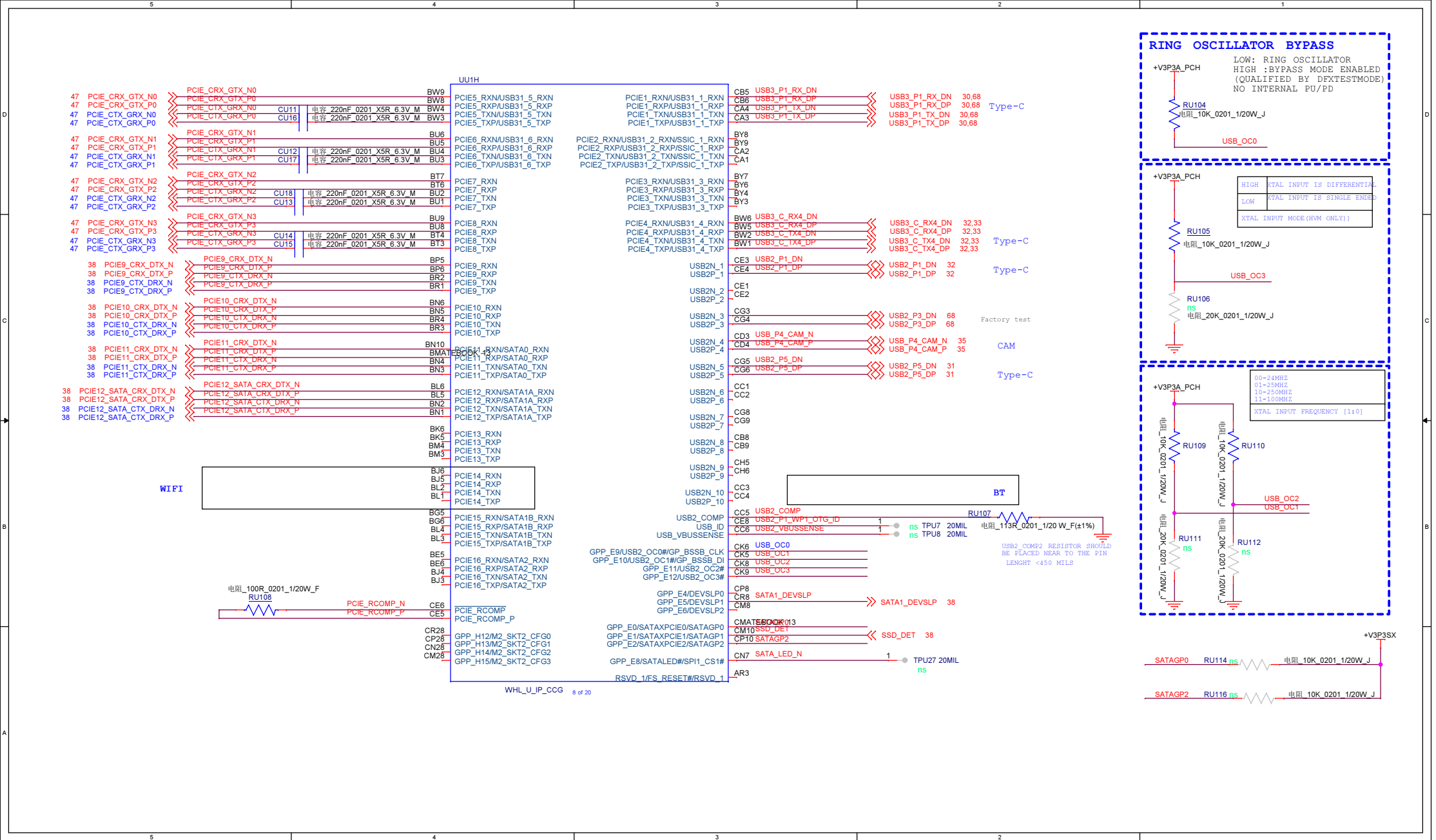


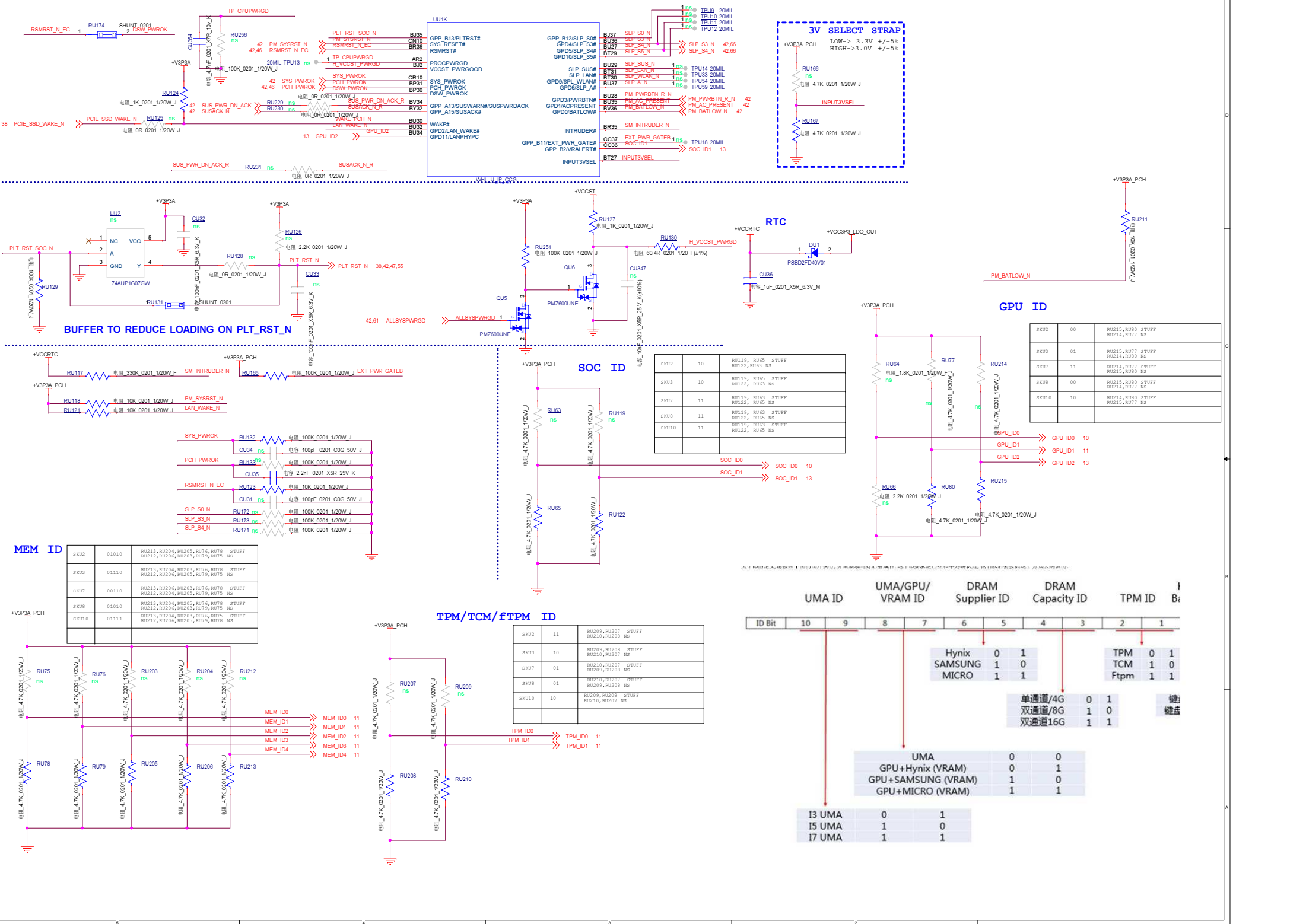
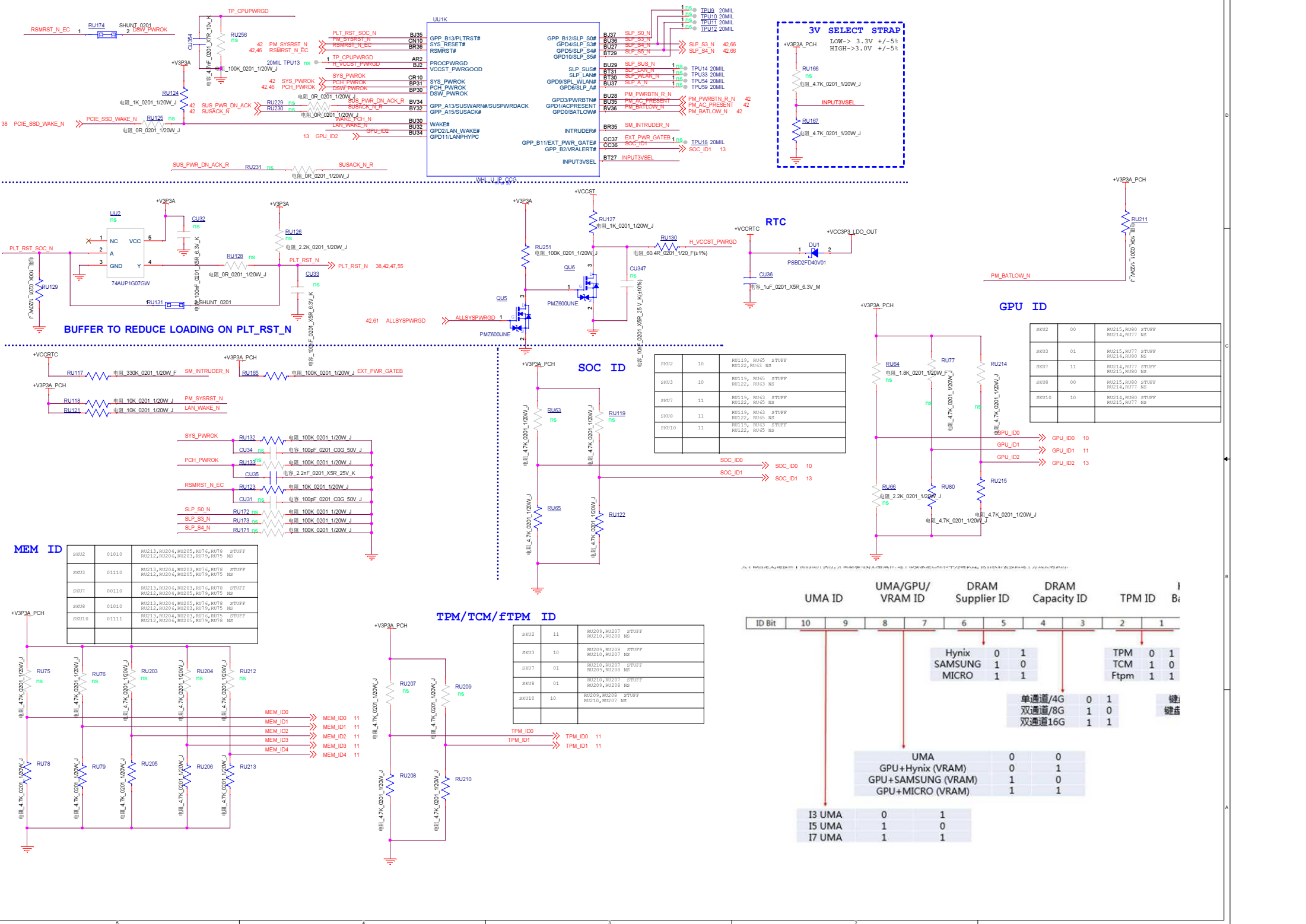
DISPLAY PORT STRAP

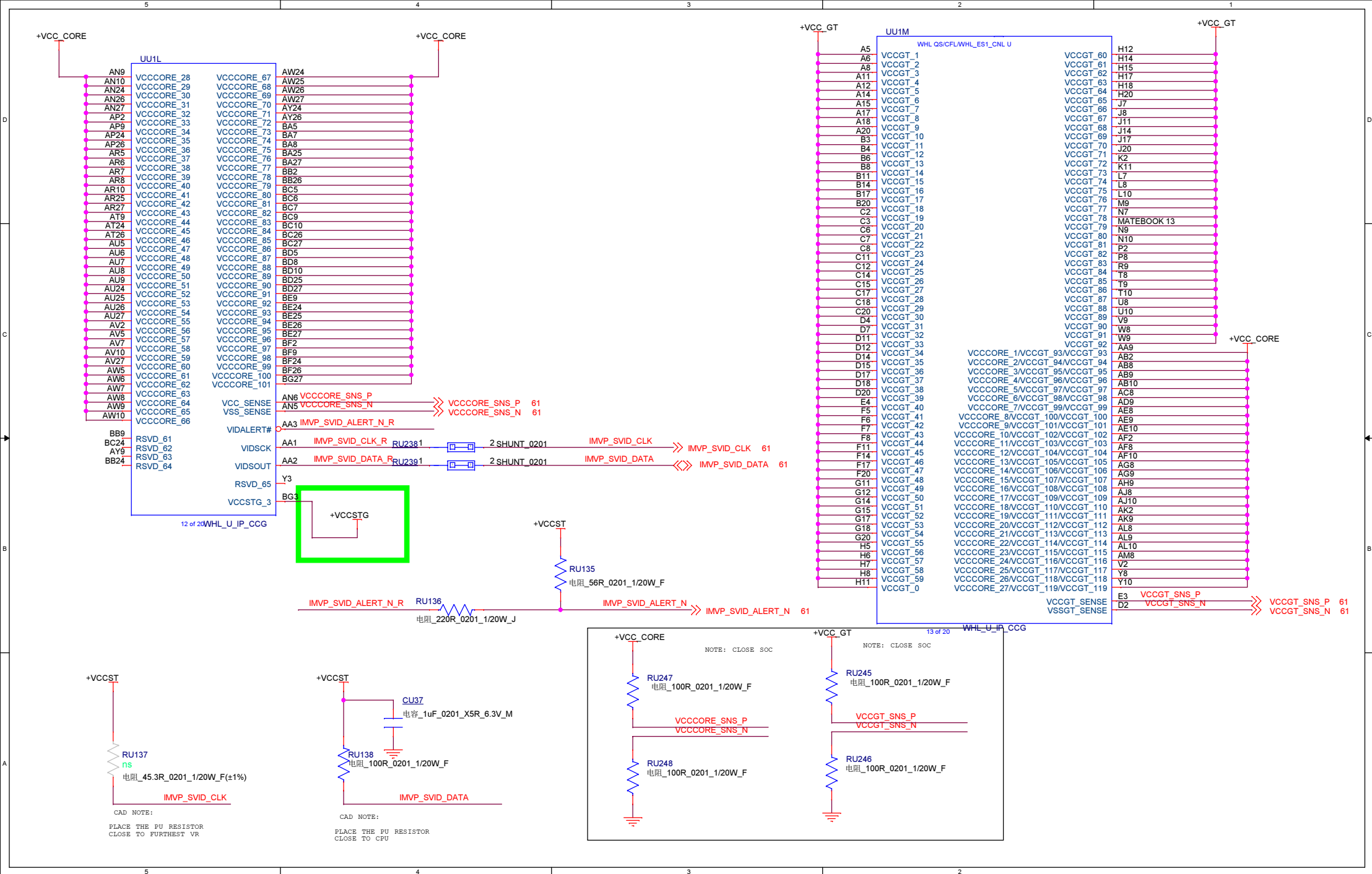
Strap	How to Enable Port	How to Disable Port	Matched HPD	DISP_RCOMP
DDI Port 1 DDPB_CTRLDATA	Pull up to 3.3 V With 2.2K	No Connect(default)	DDPB_HPD0	DISPLAY (HDMI/eDP*/DisplayPort*) 24.9Ω ± 1% to VCC0
DDI Port 2 DDPC_CTRLDATA	Pull up to 3.3 V With 2.2K (default)	No Connect	DDPC_HPD1	
eDP Port NA	NA	NA	EDP_HPD	

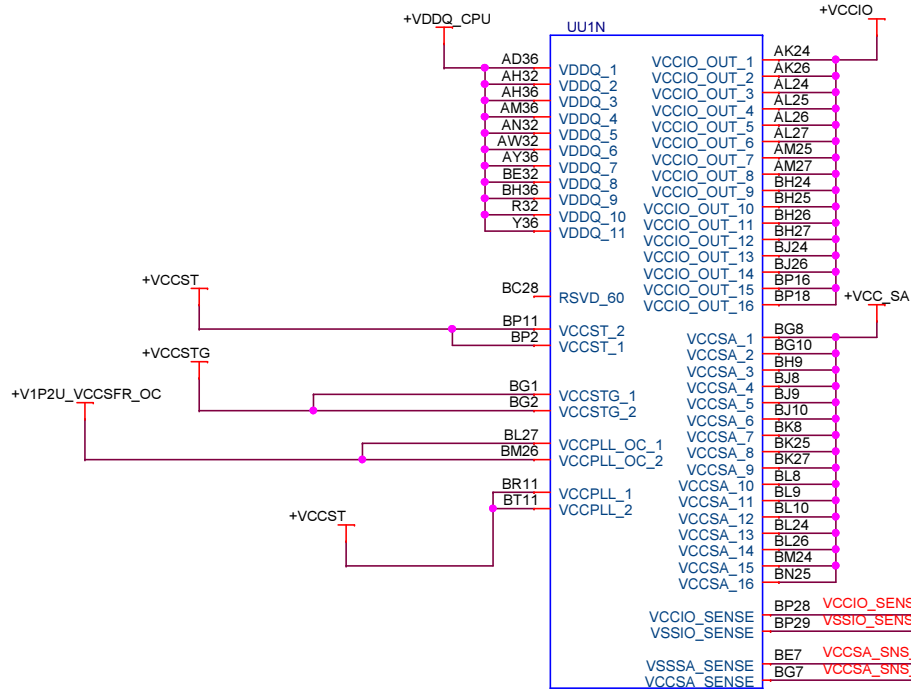
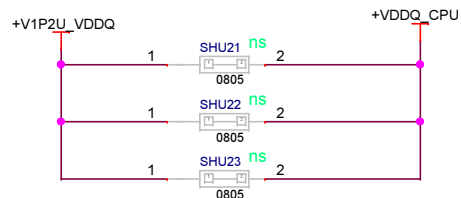






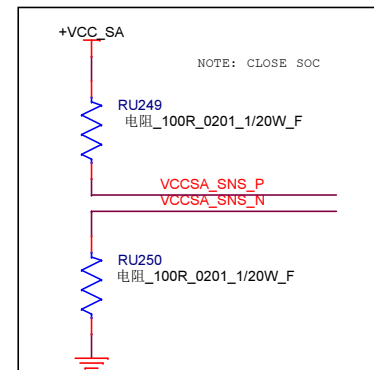


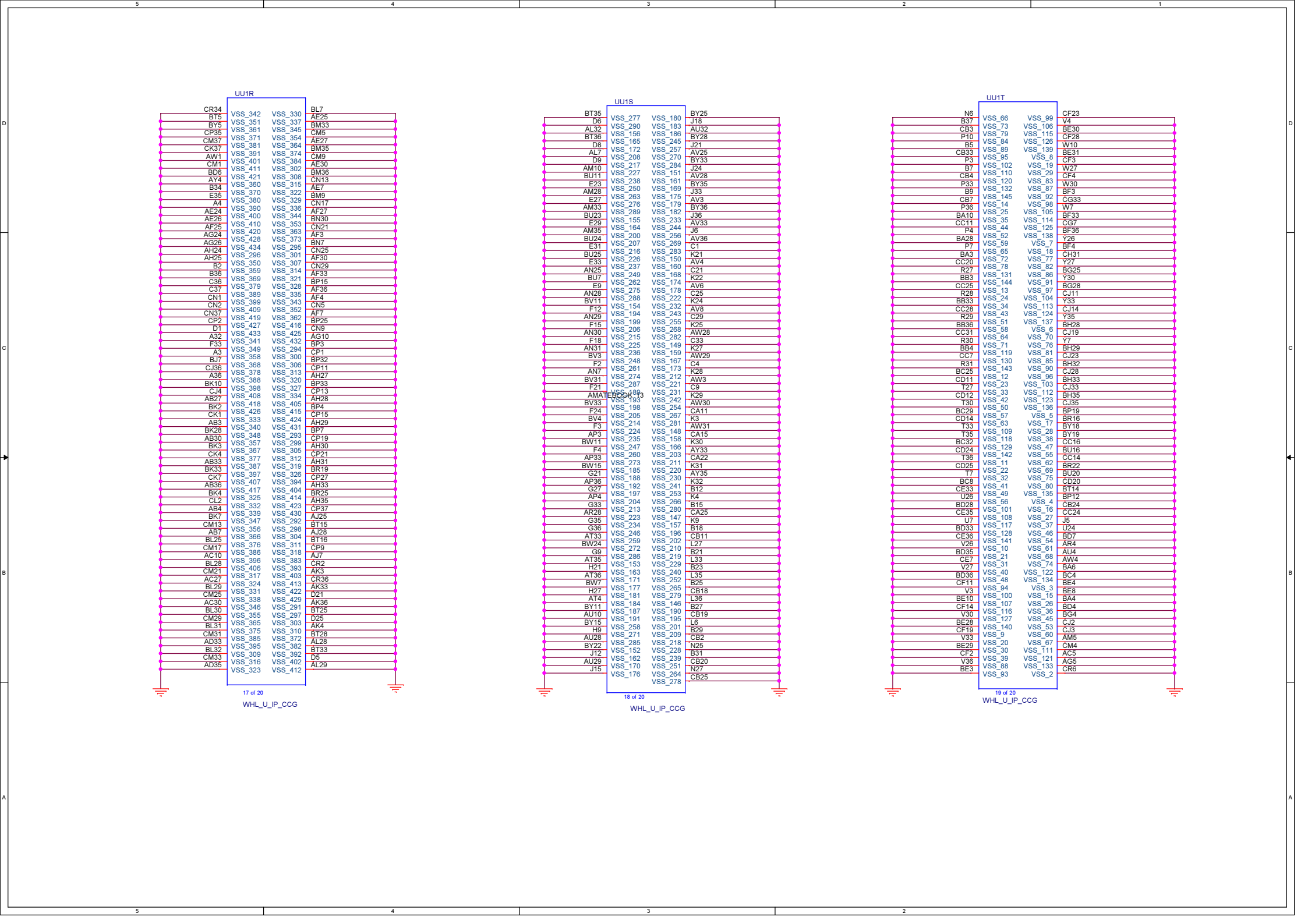


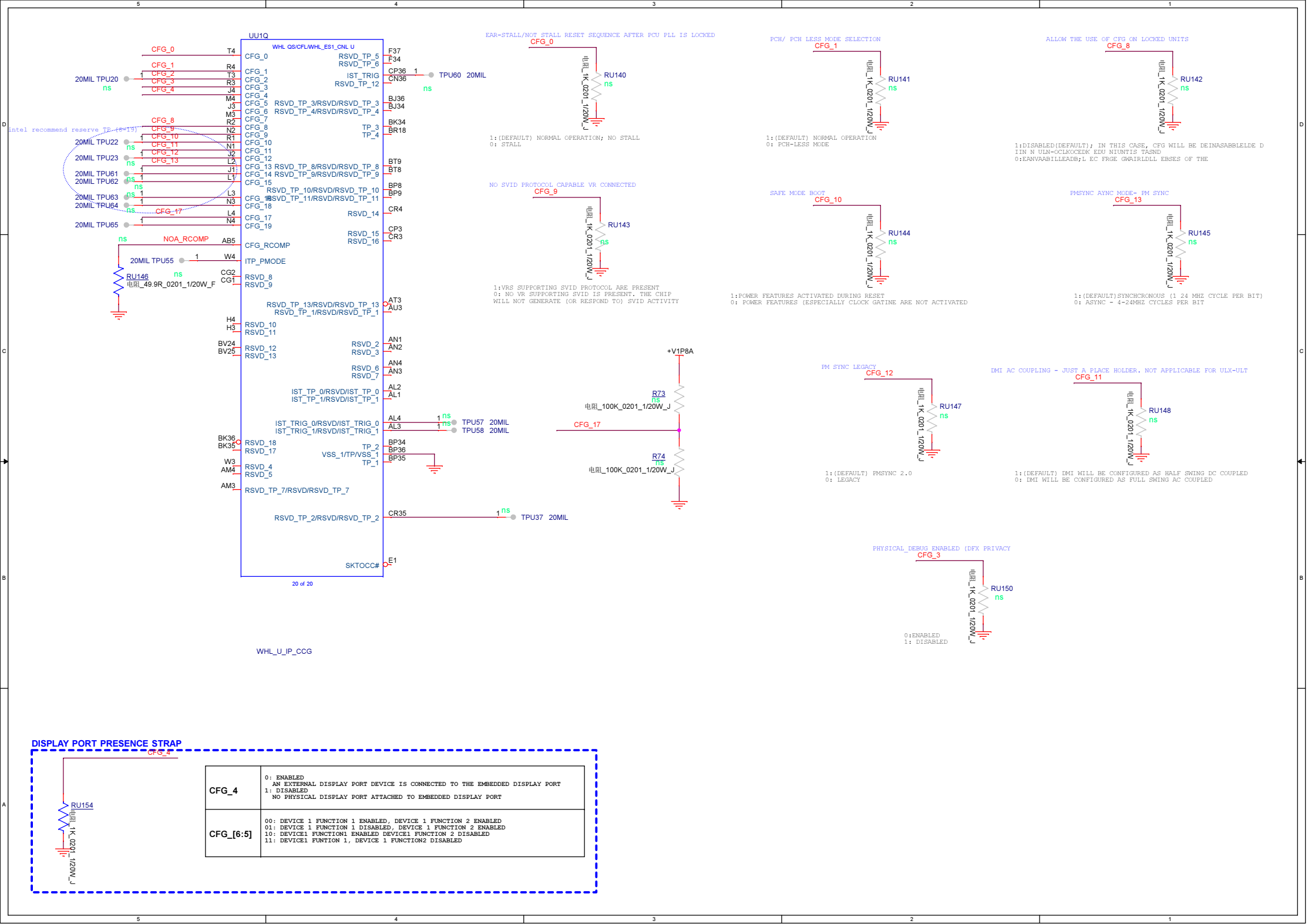


UU1O			
WHL QS/CFL UWWHL ES1_CNL U23WHL QS/CFL UWWHL ES1_CNL U22			
K12	RSVD_25/VCC_OPC_1/RSVD_25	RSVD_39/VCC_OPCIO_1/RSVD_39	AA24
K14	RSVD_26/VCC_OPC_2/RSVD_26	RSVD_40/VCC_OPCIO_2/RSVD_40	AA26
K15	RSVD_27/VCC_OPC_3/RSVD_27	RSVD_41/VCC_OPCIO_3/RSVD_41	AB25
K17	RSVD_28/VCC_OPC_4/RSVD_28	RSVD_42/VCC_OPCIO_4/RSVD_42	AC24
K18	RSVD_29/VCC_OPC_5/RSVD_29	RSVD_43/VCC_OPCIO_5/RSVD_43	AC25
K20	RSVD_30/VCC_OPC_6/RSVD_30	RSVD_44/VCC_OPCIO_6/RSVD_44	AC26
L25	RSVD_31/VCC_OPC_7/RSVD_31	RSVD_45/VCC_OPCIO_7/RSVD_45	AD24
M24	RSVD_32/VCC_OPC_8/RSVD_32	RSVD_46/VCC_OPCIO_8/RSVD_46	AD26
M26	RSVD_33/VCC_OPC_9/RSVD_23/RSVD_19/VCC_OPCIO_SENSE/RSVD_19	RSVD_56	V25
P24	RSVD_34/VCC_OPC_10/RSVD_34/RSVD_20/VCC_OPCIO_SENSE/RSVD_20	RSVD_57	T25
P26	RSVD_35/VCC_OPC_11/RSVD_35	RSVD_58/OPC_RCOMP/RSVD_58	A35
R24	RSVD_36/VCC_OPC_12/RSVD_36		D34
R25	RSVD_37/VCC_OPC_13/RSVD_37		N5
R26	RSVD_38/VCC_OPC_14/RSVD_38		
V24	RSVD_21/VCC_OPC_1P8_3/RSVD_21		
V25	RSVD_22/VCC_OPC_1P8_4/RSVD_22		
Y24	RSVD_23/VCC_OPC_1P8_1/RSVD_23		
Y25	RSVD_24/VCC_OPC_1P8_2/RSVD_24		
G2	RSVD_47		
G1	RSVD_48		
C34	RSVD_49/VSS_435/RSVD_49		
G3	RSVD_50/VSS_436/RSVD_50		
G4	RSVD_51/VSS_437/RSVD_51		
A34	RSVD_52/RSVD_TP/RSVD_52		
B35	RSVD_53/RSVD_TP/RSVD_53		
AJ27	RSVD_54/MSM#/RSVD_54		
AH26	RSVD_55/ZVM#/RSVD_55		
L5	RSVD_59/OPCE_RCOMP/RSVD_59		

WHL_U_IP_CCG

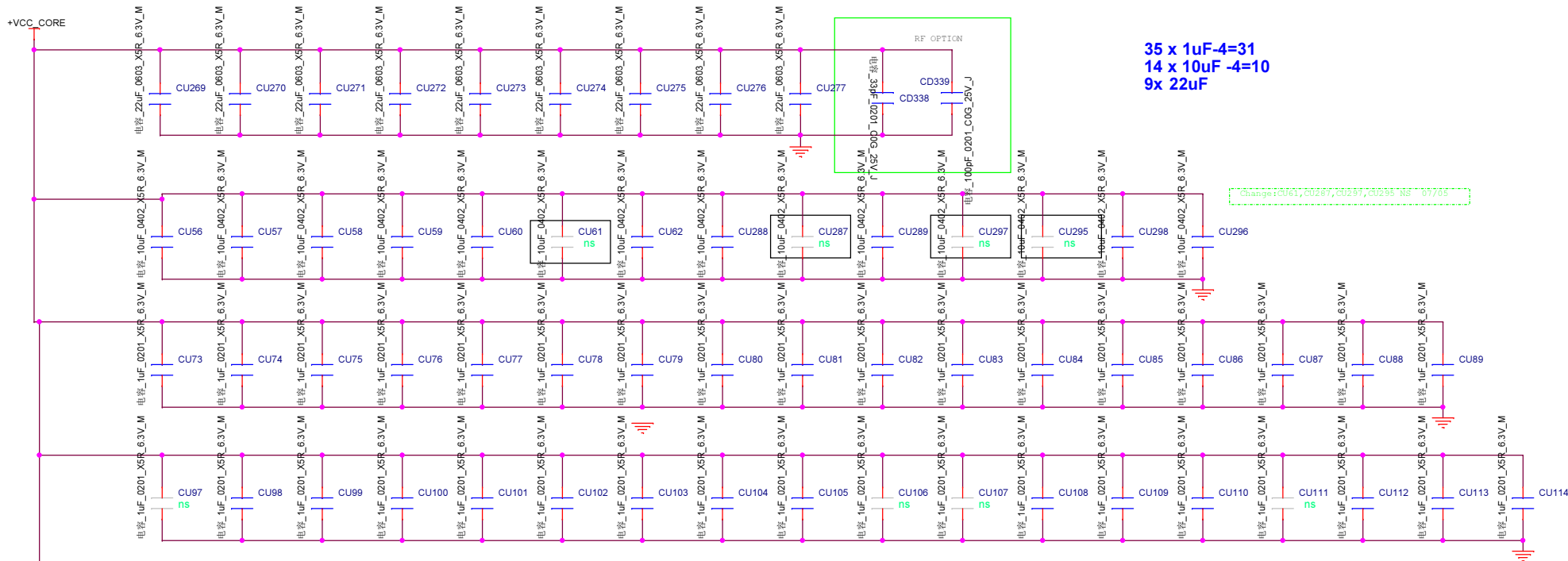






PLACE THESE CAPS UNDERNEATH BGA AREA

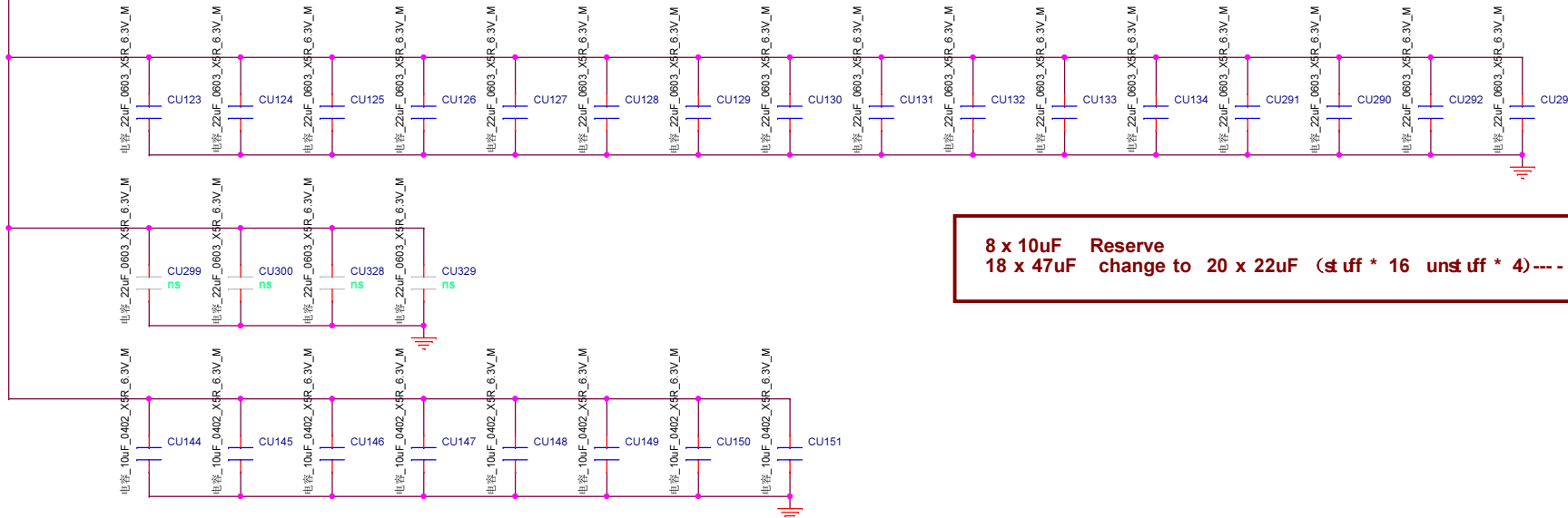
+VCCCORE



35 x 1uF-4=31
14 x 10uF -4=10
9x 22uF

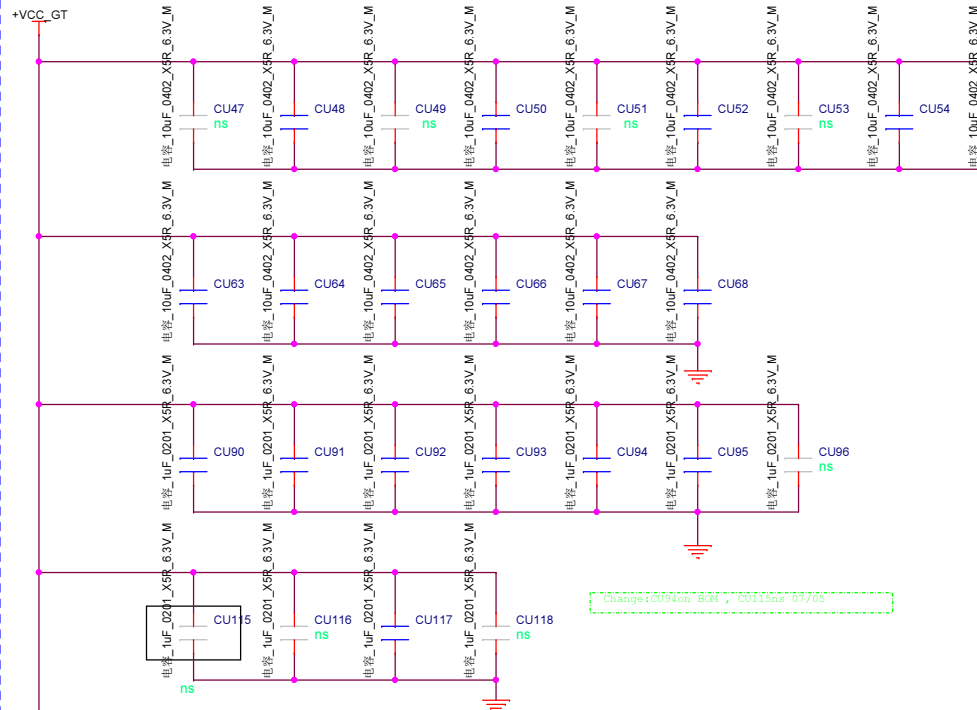
CD339, CD338, CD337, CD336, CD335, CD334, CD333, CD332, CD331, CD330, CD329, CD328, CD327, CD326, CD325, CD324, CD323, CD322, CD321, CD320, CD319, CD318, CD317, CD316, CD315, CD314, CD313, CD312, CD311, CD310, CD309, CD308, CD307, CD306, CD305, CD304, CD303, CD302, CD301, CD300, CD299, CD298, CD297, CD296, CD295, CD294, CD293, CD292, CD291, CD290, CD289, CD288, CD287, CD286, CD285, CD284, CD283, CD282, CD281, CD280, CD279, CD278, CD277, CD276, CD275, CD274, CD273, CD272, CD271, CD270, CD269, CD268, CD267, CD266, CD265, CD264, CD263, CD262, CD261, CD260, CD259, CD258, CD257, CD256, CD255, CD254, CD253, CD252, CD251, CD250, CD249, CD248, CD247, CD246, CD245, CD244, CD243, CD242, CD241, CD240, CD239, CD238, CD237, CD236, CD235, CD234, CD233, CD232, CD231, CD230, CD229, CD228, CD227, CD226, CD225, CD224, CD223, CD222, CD221, CD220, CD219, CD218, CD217, CD216, CD215, CD214, CD213, CD212, CD211, CD210, CD209, CD208, CD207, CD206, CD205, CD204, CD203, CD202, CD201, CD200, CD199, CD198, CD197, CD196, CD195, CD194, CD193, CD192, CD191, CD190, CD189, CD188, CD187, CD186, CD185, CD184, CD183, CD182, CD181, CD180, CD179, CD178, CD177, CD176, CD175, CD174, CD173, CD172, CD171, CD170, CD169, CD168, CD167, CD166, CD165, CD164, CD163, CD162, CD161, CD160, CD159, CD158, CD157, CD156, CD155, CD154, CD153, CD152, CD151, CD150, CD149, CD148, CD147, CD146, CD145, CD144, CD143, CD142, CD141, CD140, CD139, CD138, CD137, CD136, CD135, CD134, CD133, CD132, CD131, CD130, CD129, CD128, CD127, CD126, CD125, CD124, CD123, CD122, CD121, CD120, CD119, CD118, CD117, CD116, CD115, CD114, CD113, CD112, CD111, CD110, CD109, CD108, CD107, CD106, CD105, CD104, CD103, CD102, CD101, CD100, CD99, CD98, CD97, CD96, CD95, CD94, CD93, CD92, CD91, CD90, CD89, CD88, CD87, CD86, CD85, CD84, CD83, CD82, CD81, CD80, CD79, CD78, CD77, CD76, CD75, CD74, CD73, CD72, CD71, CD70, CD69, CD68, CD67, CD66, CD65, CD64, CD63, CD62, CD61, CD60, CD59, CD58, CD57, CD56, CD55, CD54, CD53, CD52, CD51, CD50, CD49, CD48, CD47, CD46, CD45, CD44, CD43, CD42, CD41, CD40, CD39, CD38, CD37, CD36, CD35, CD34, CD33, CD32, CD31, CD30, CD29, CD28, CD27, CD26, CD25, CD24, CD23, CD22, CD21, CD20, CD19, CD18, CD17, CD16, CD15, CD14, CD13, CD12, CD11, CD10, CD9, CD8, CD7, CD6, CD5, CD4, CD3, CD2, CD1, CD0

PLACE CLOSE TO PACKAGE ON PRIMARY SIDE

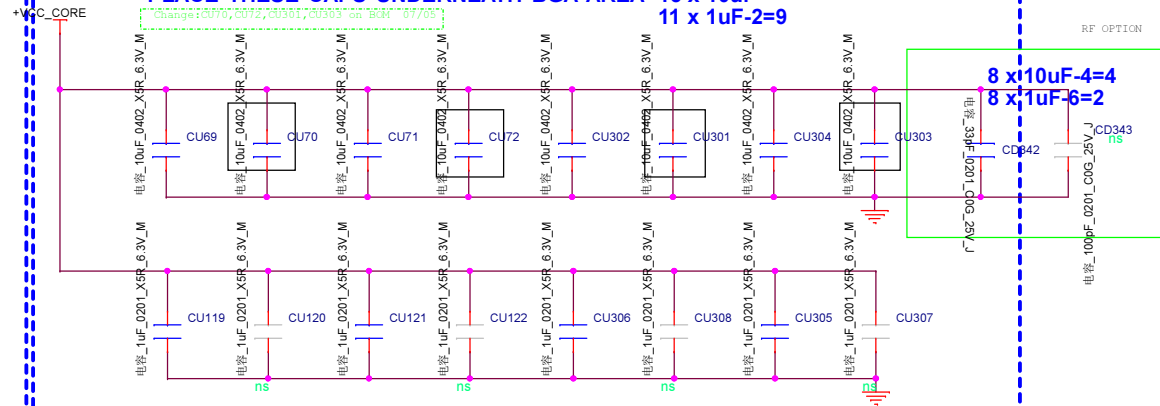


8 x 10uF Reserve
18 x 47uF change to 20 x 22uF (st uff * 16 unst uff * 4) --- 01/5

PLACE THESE CAPS UNDERNEATH BGA AREA

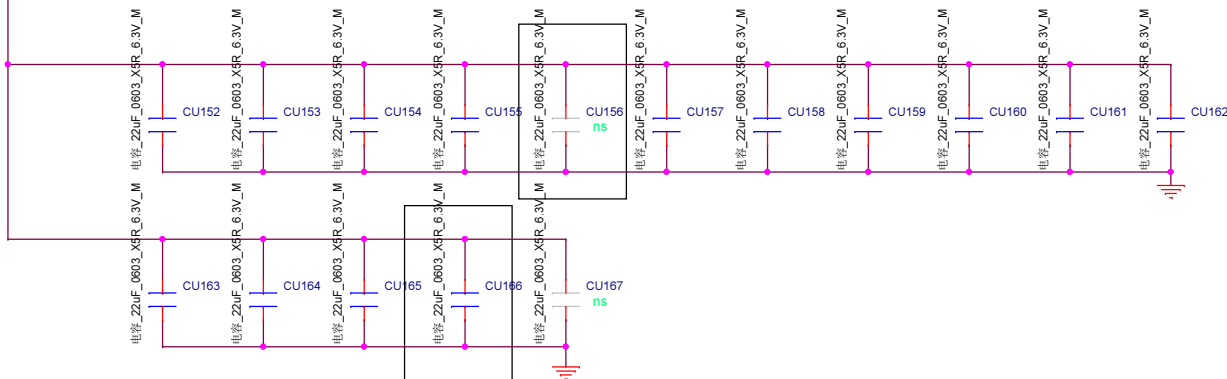


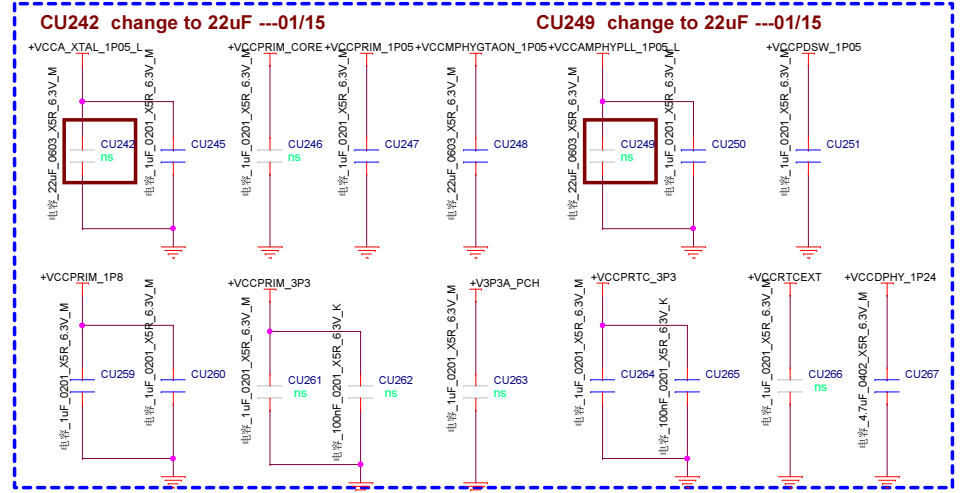
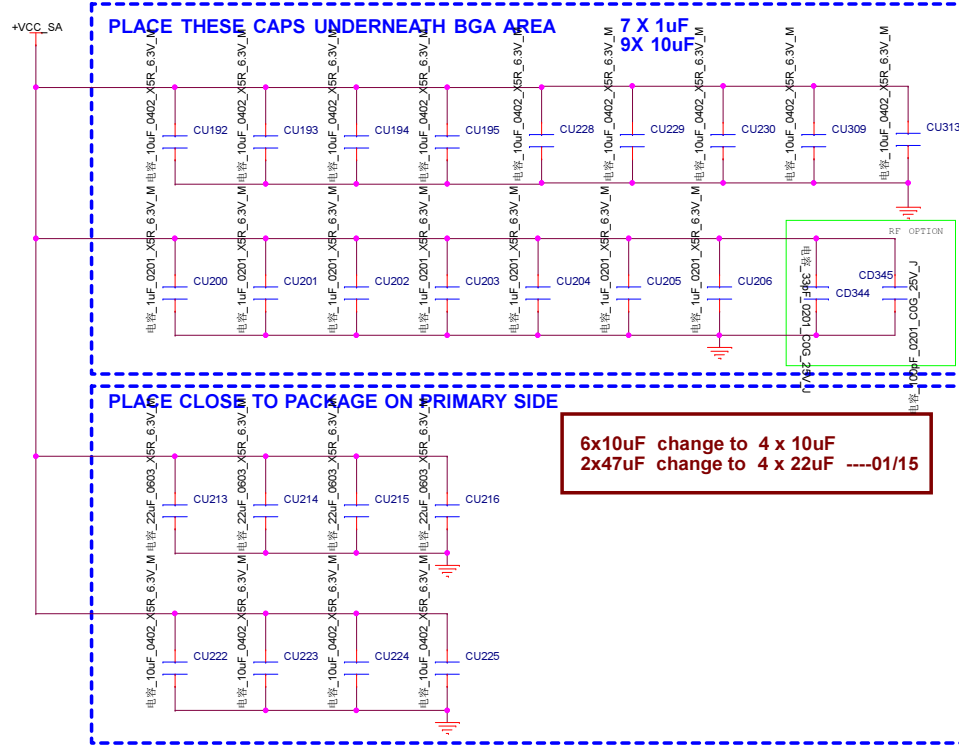
PLACE THESE CAPS UNDERNEATH BGA AREA

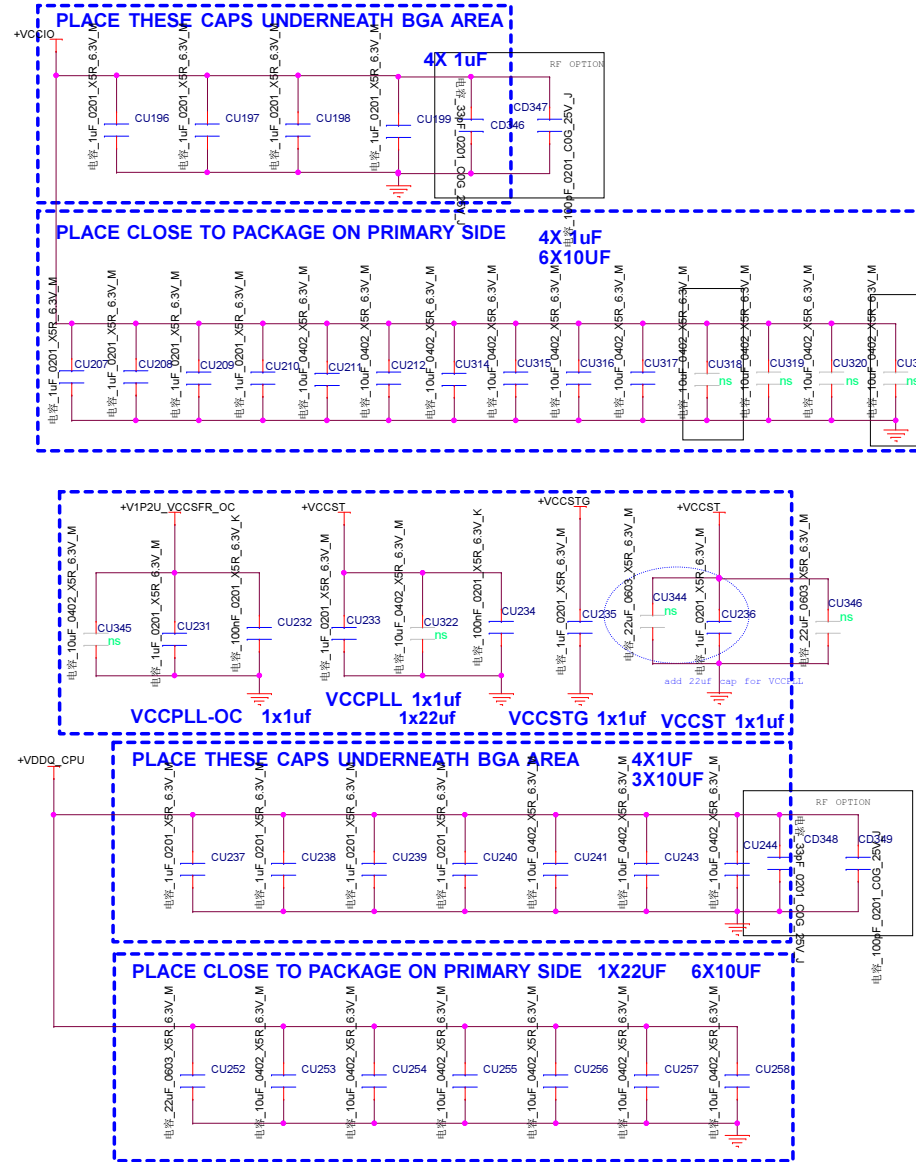


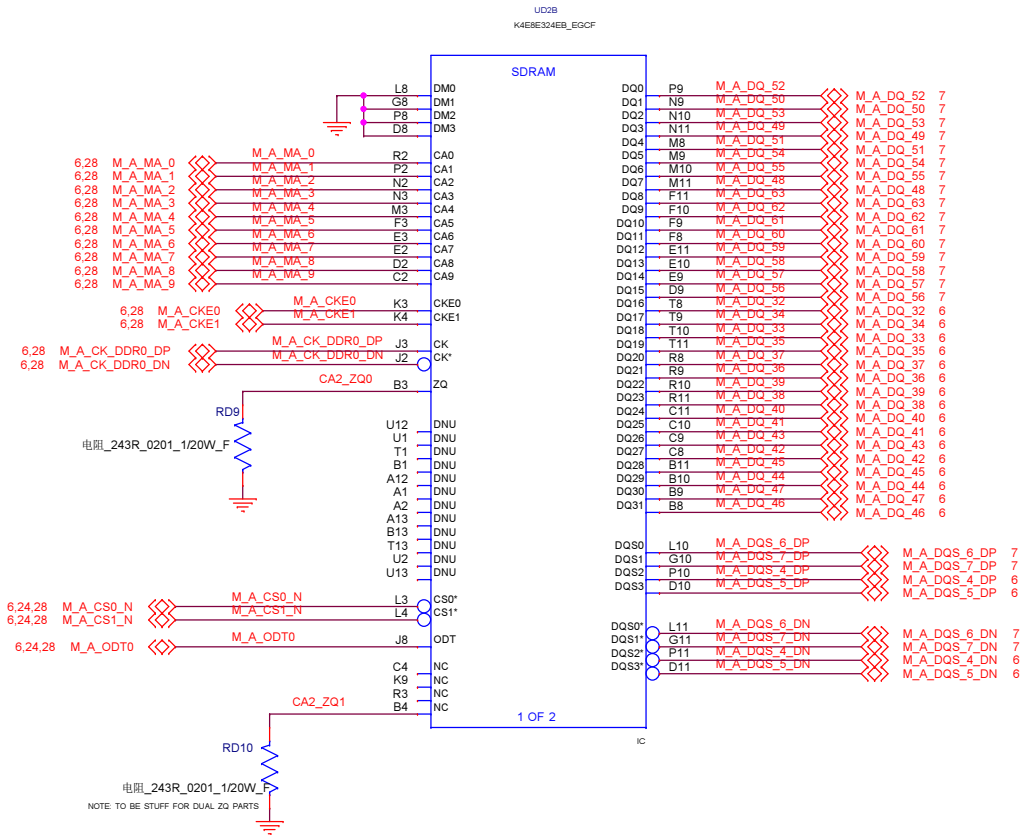
PLACE CLOSE TO PACKAGE ON PRIMARY SIDE

15 x 22uF change to 16 x 22uF @ 14 unstuff * 2)
8 x 47uF delete ----01/15

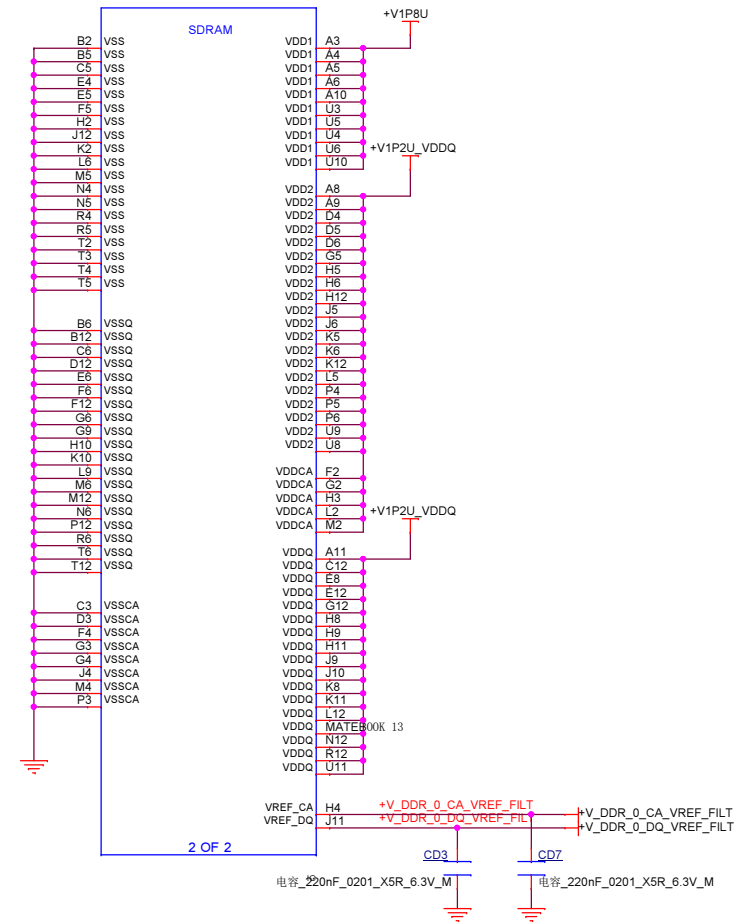


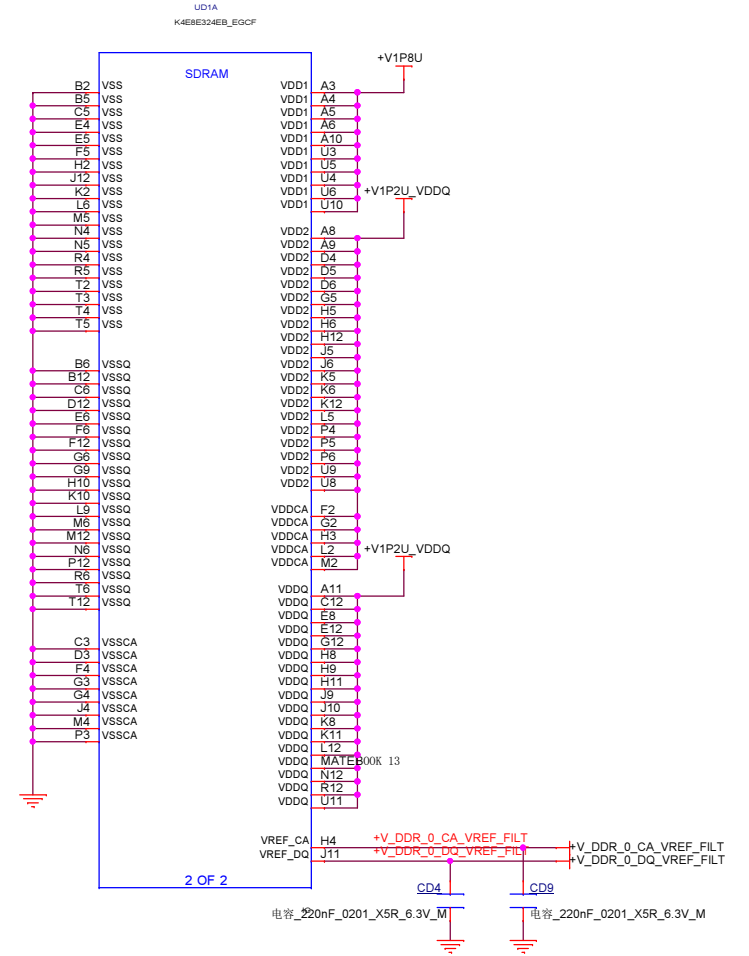
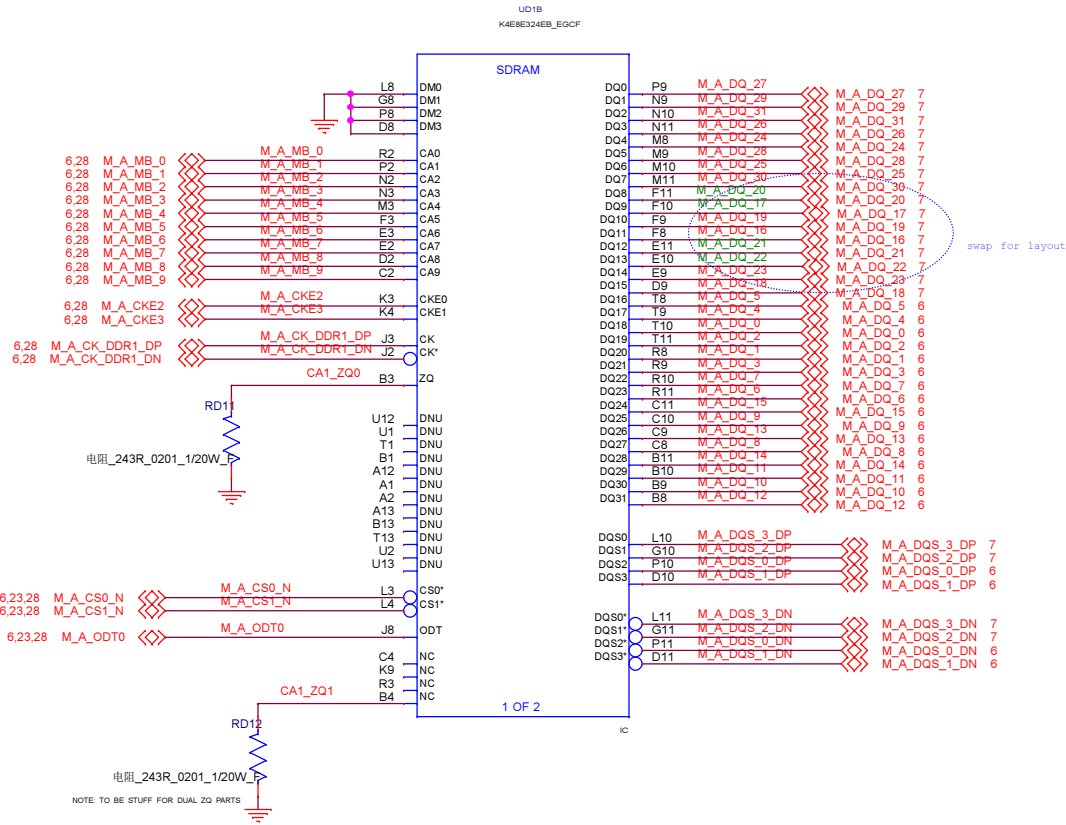


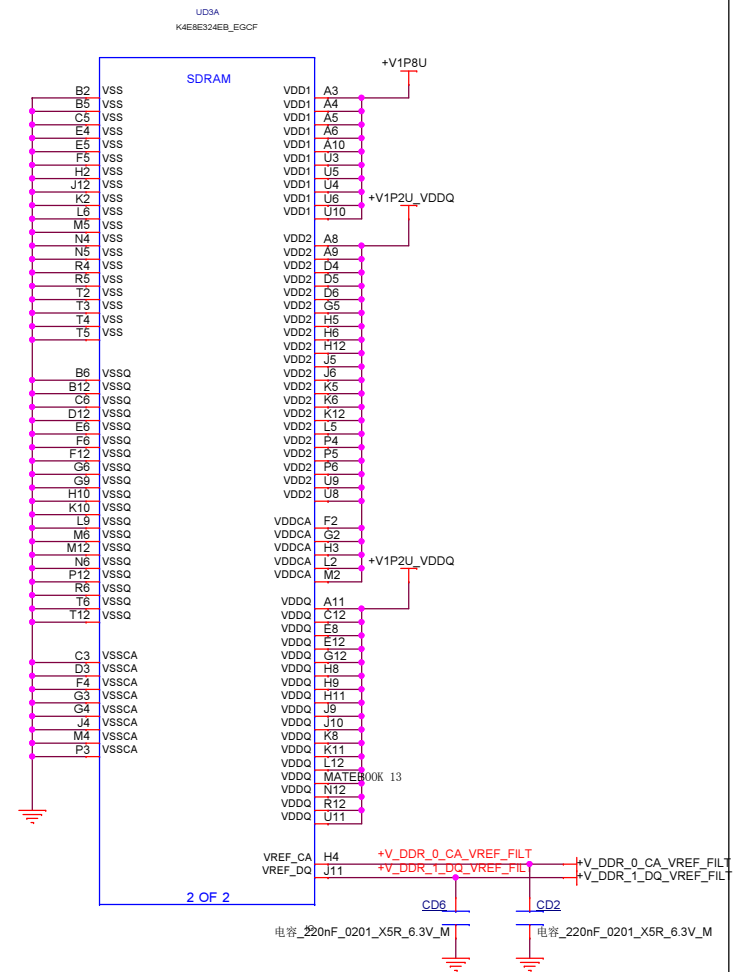
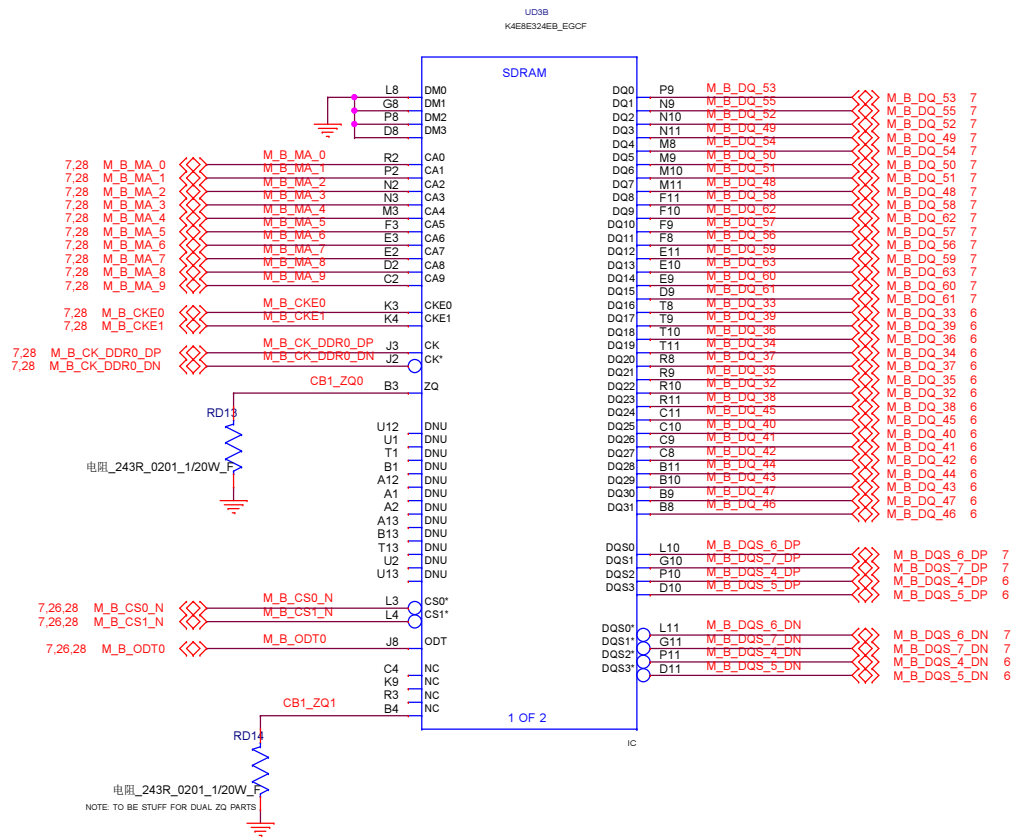


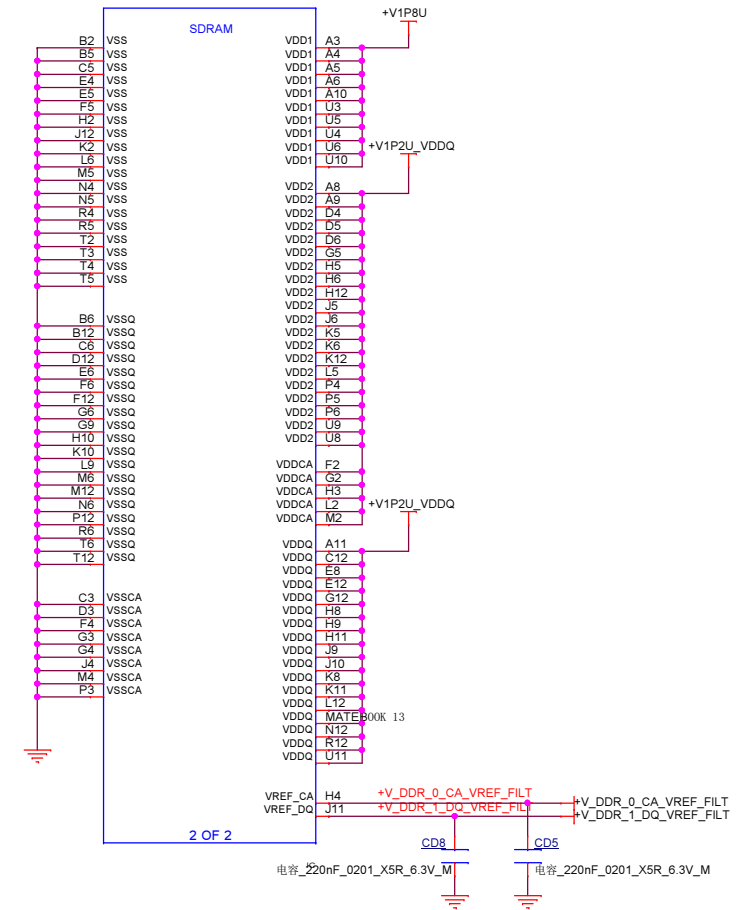
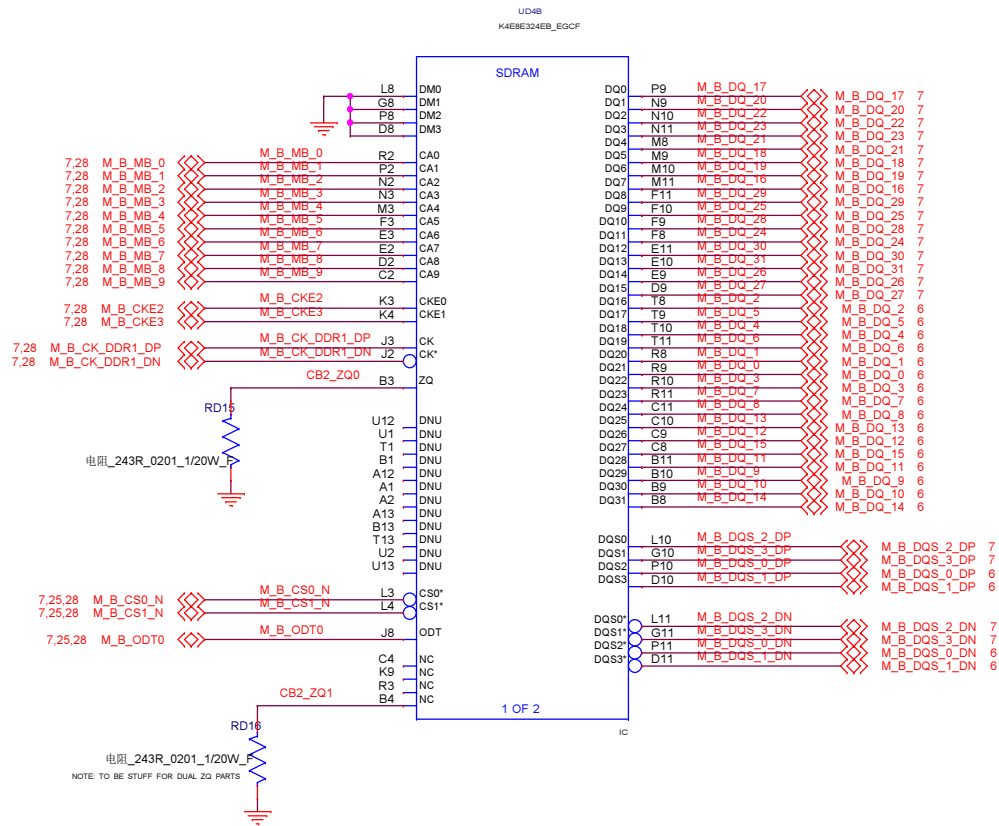


UD2A
K4E8E324EB_EGCF



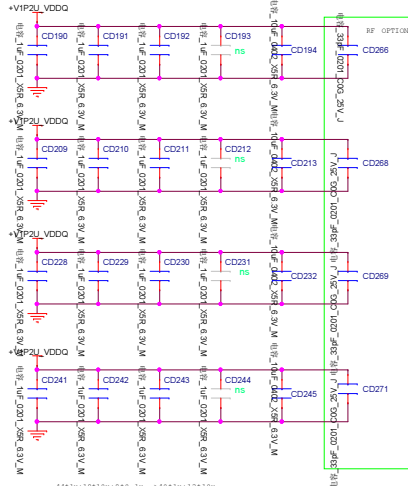




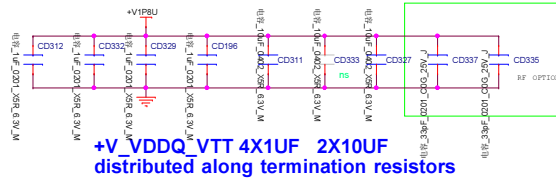


DECOUPLING CAPACITORS FOR DDR CHANNEL A

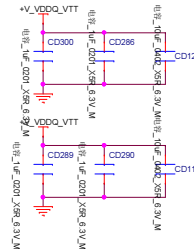
VDDQ 18X1UF-5=13 6X10UF+1=7



+V1P8U 4X1UF 3X10UF

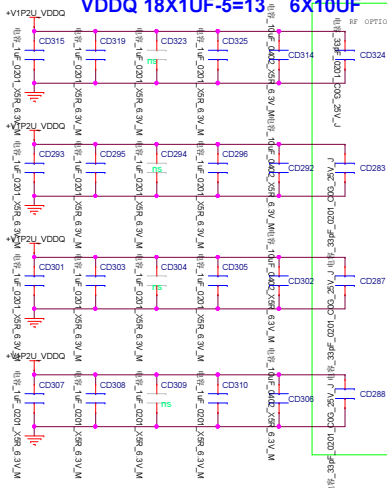


+V_VDDQ_VTT 4X1UF 2X10UF
distributed along termination resistors

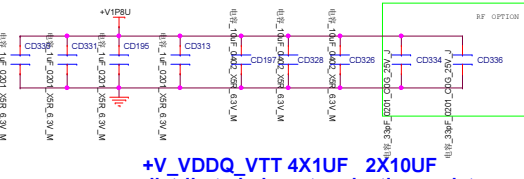


DECOUPLING CAPACITORS FOR DDR CHANNEL B

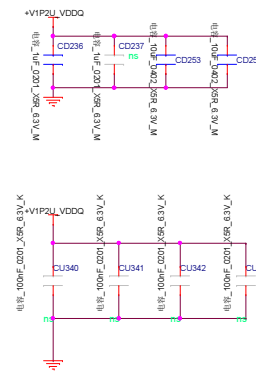
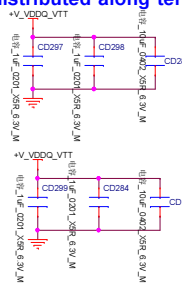
VDDQ 18X1UF-5=13 6X10UF



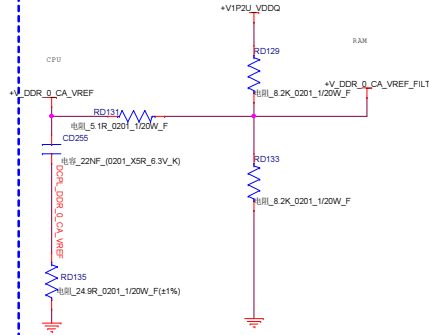
+V1P8U 4X1UF 2X10UF



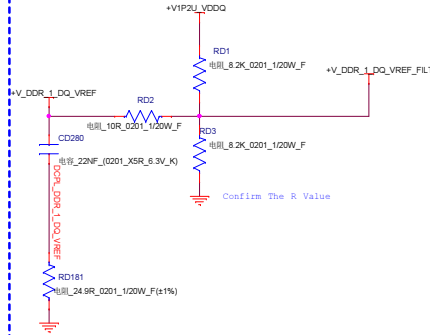
+V_VDDQ_VTT 4X1UF 2X10UF
distributed along termination resistors



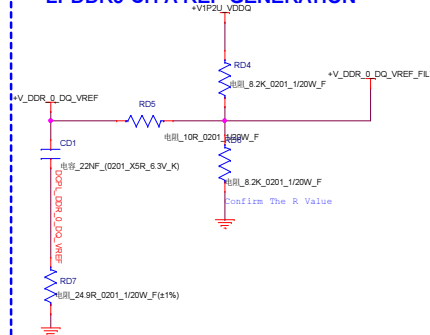
LPDDR3 CH A REF CA GENERATION



LPDDR3 CH B REF CA GENERATION



LPDDR3 CH A REF GENERATION

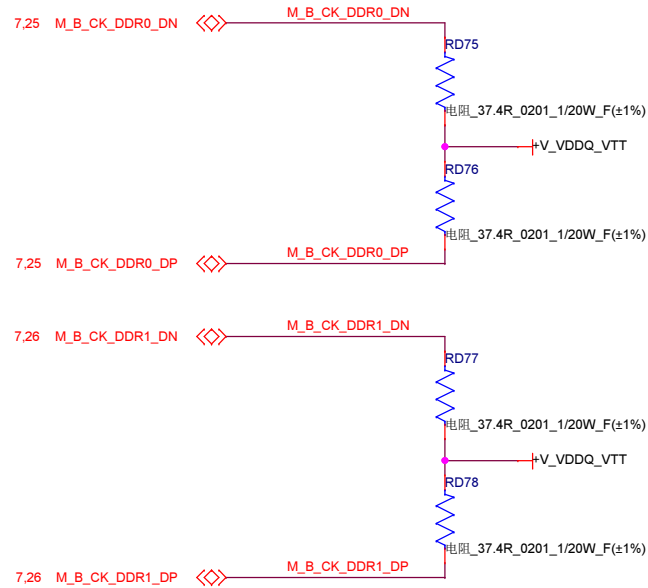
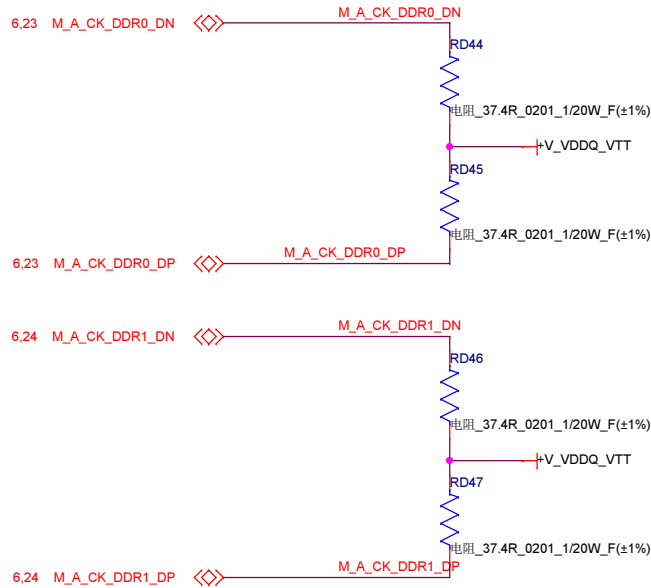
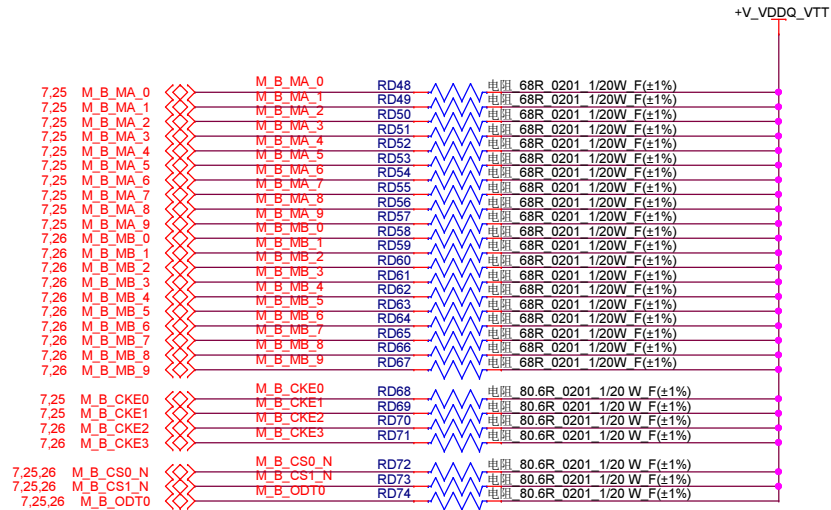
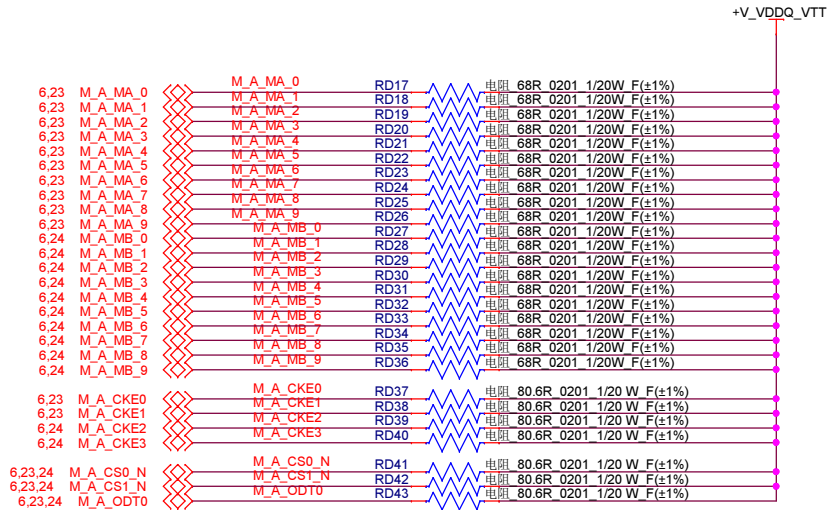


MEMORY TERMINATIONS

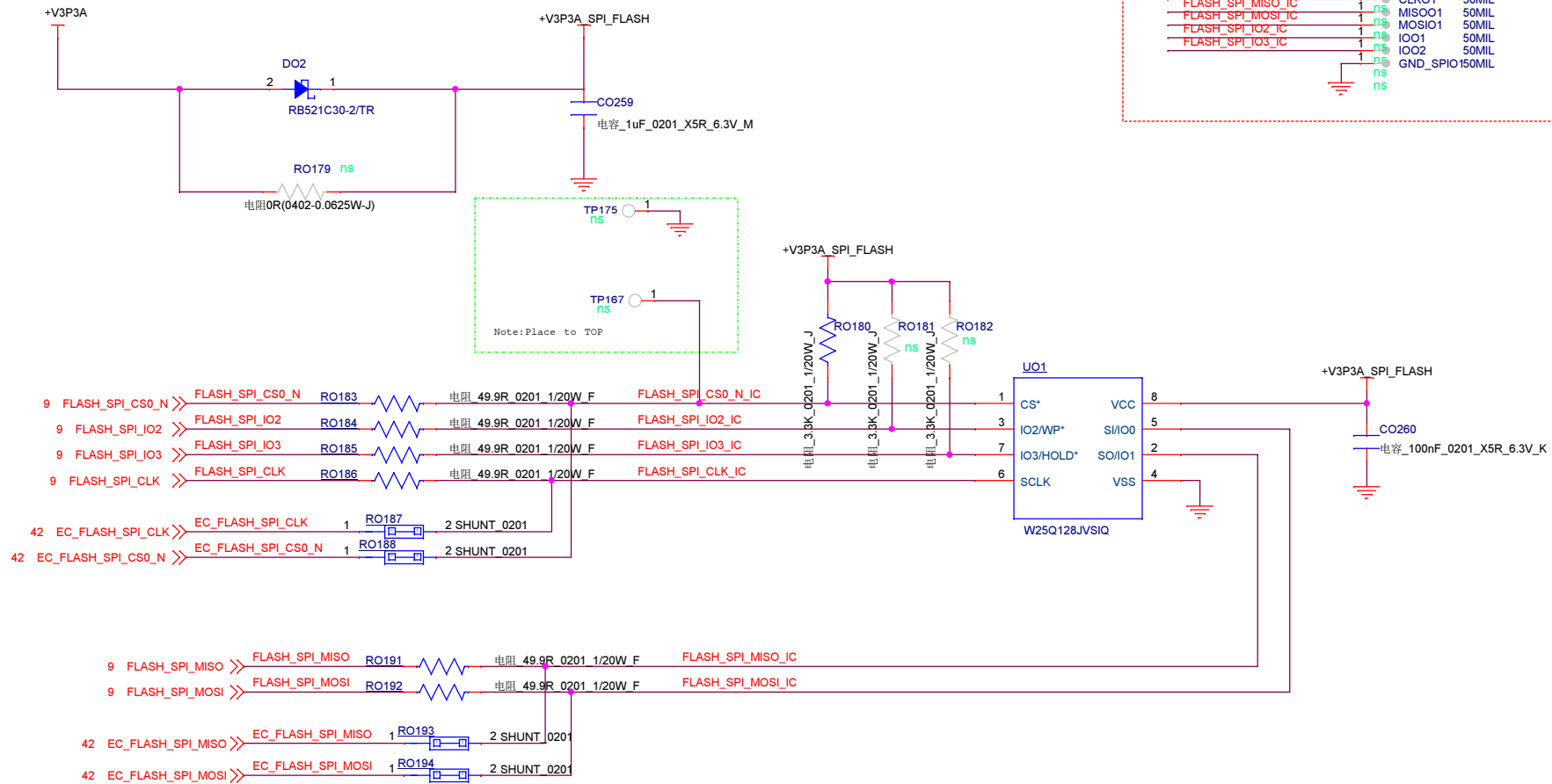
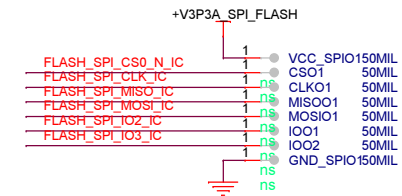
CHANNEL A

MEMORY TERMINATIONS

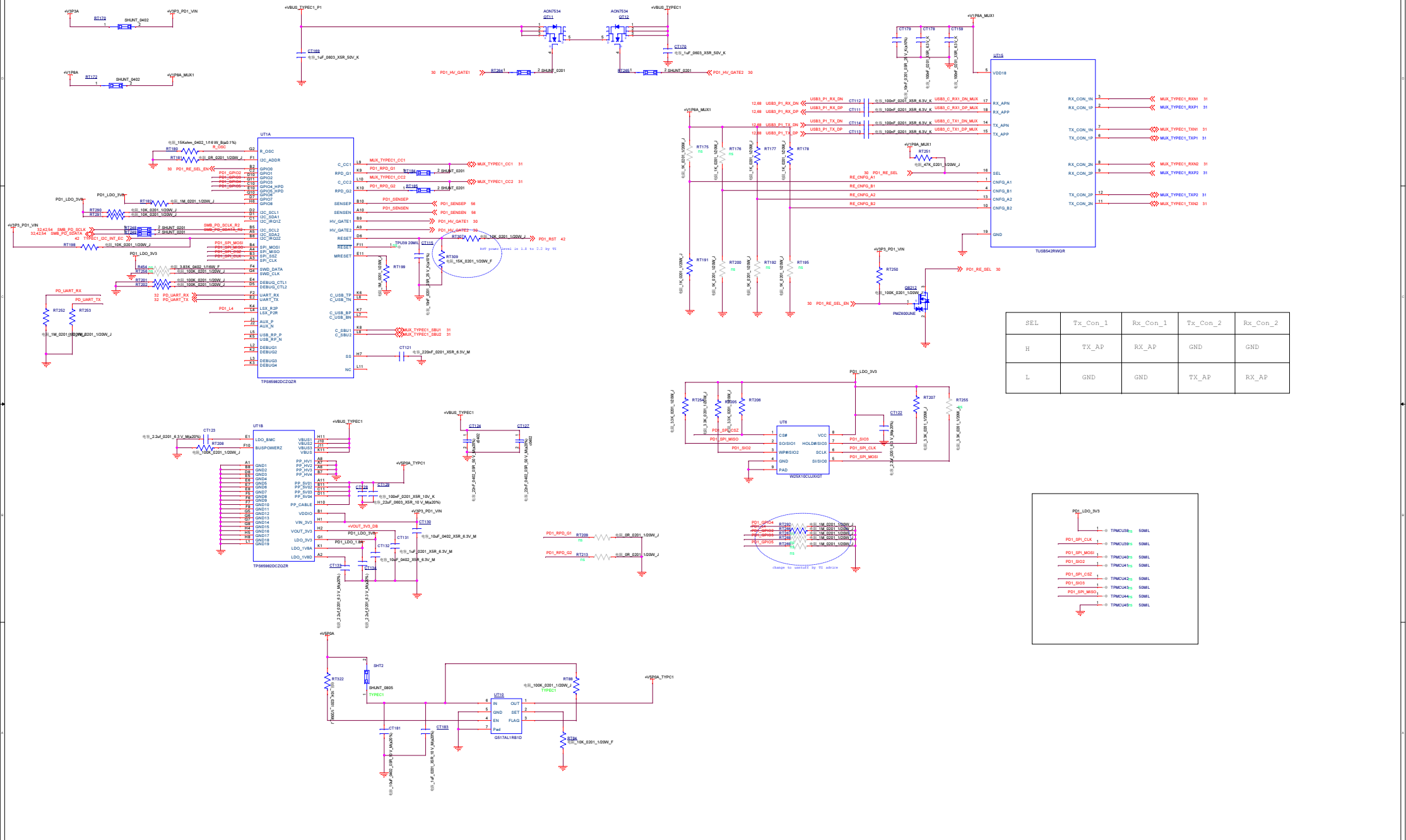
CHANNEL B

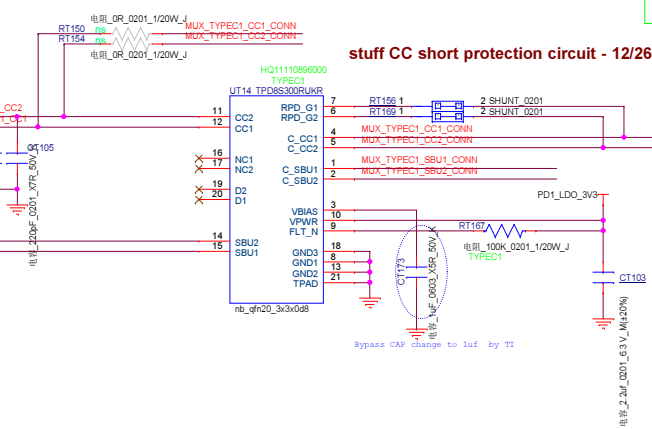
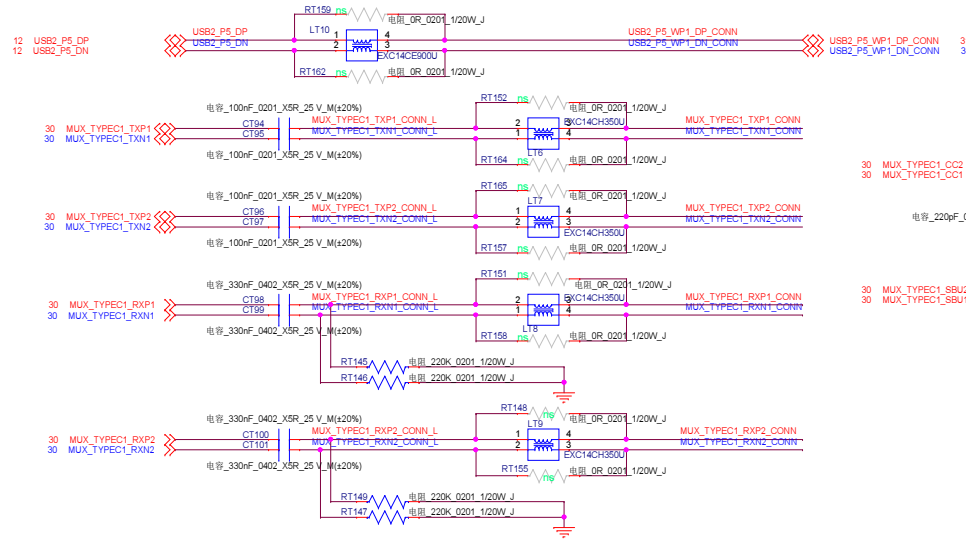


FOR product line

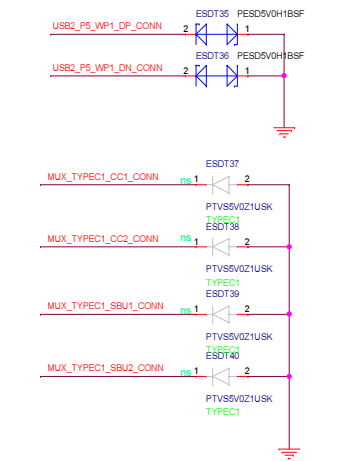
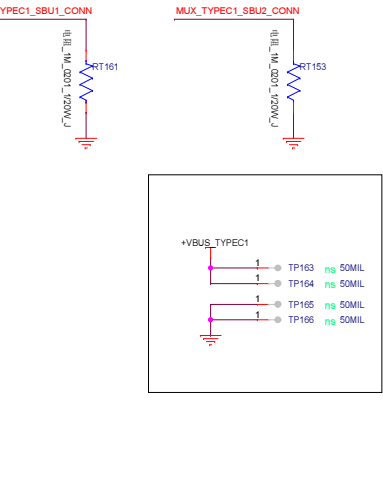
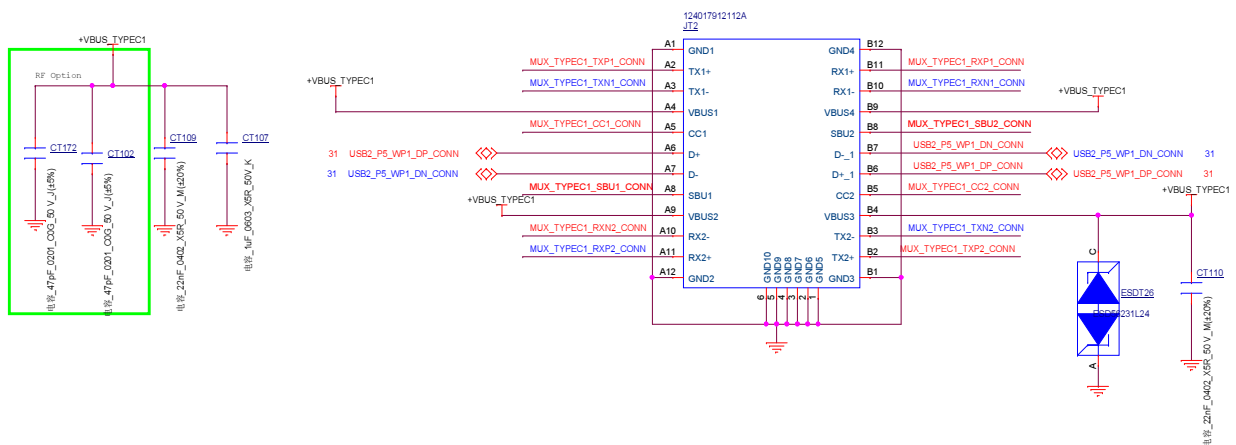
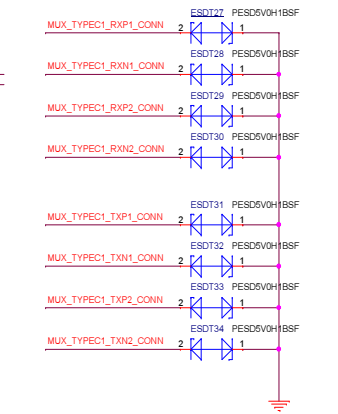
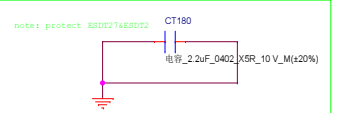


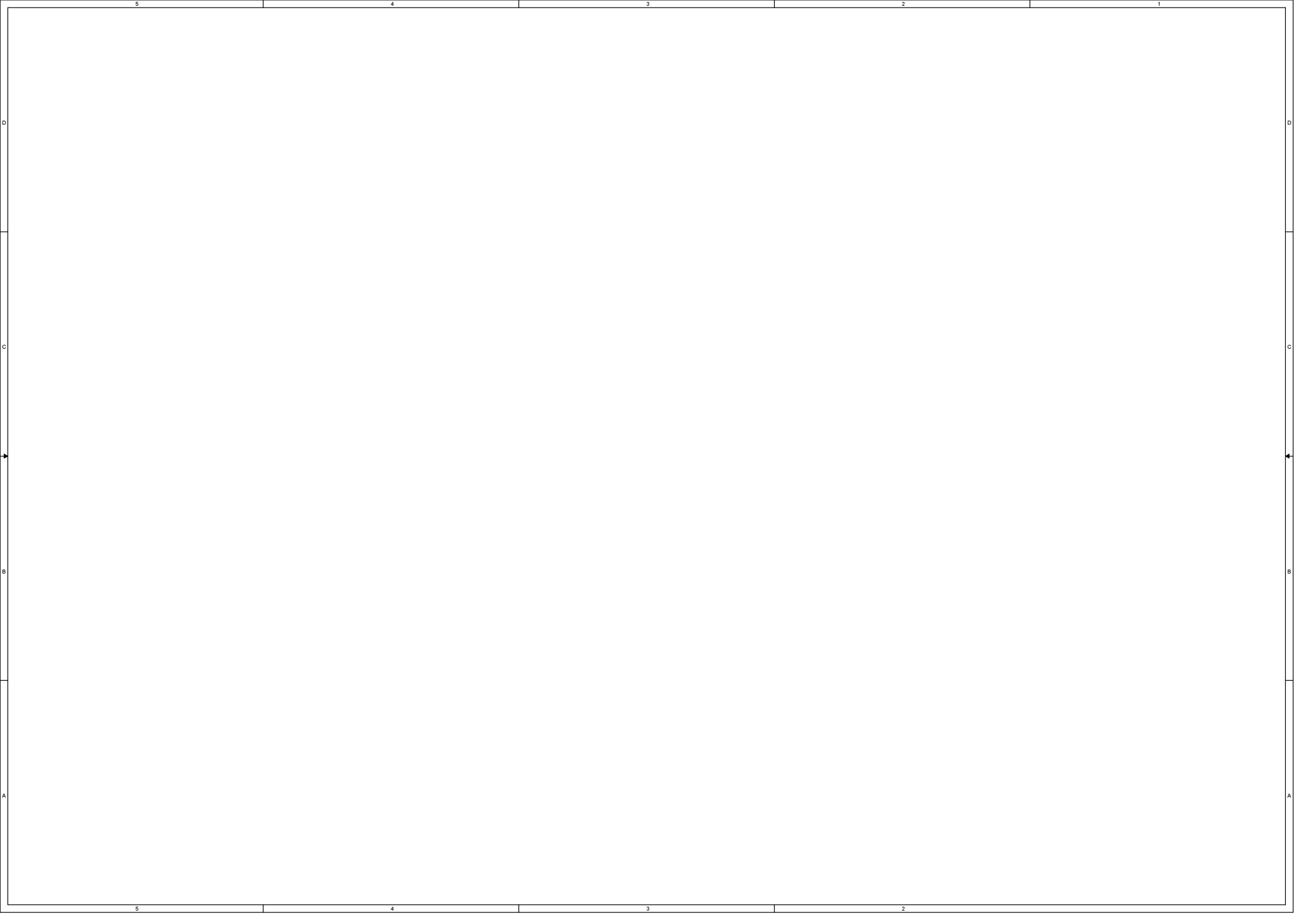
add CRT40 - 0108

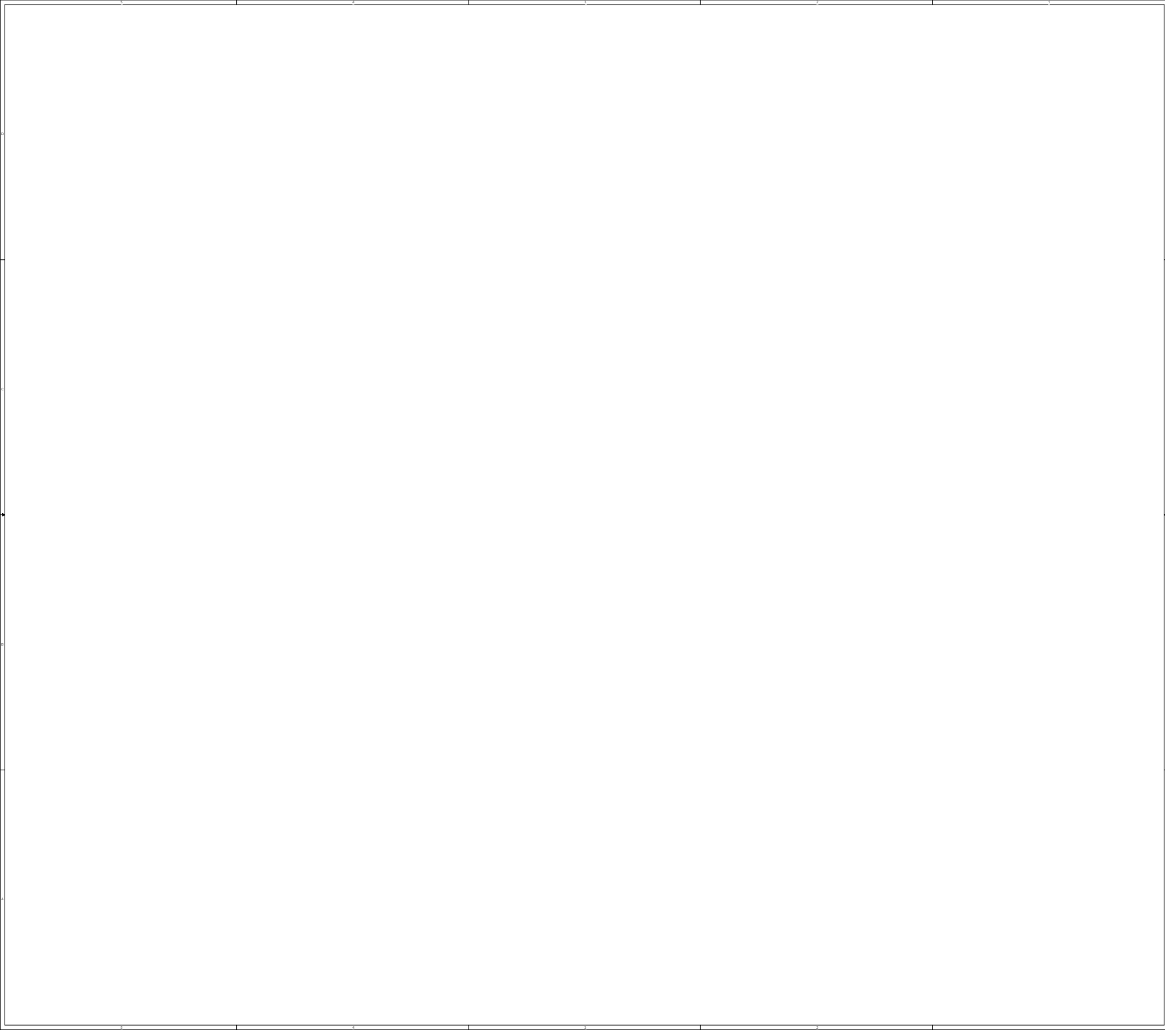




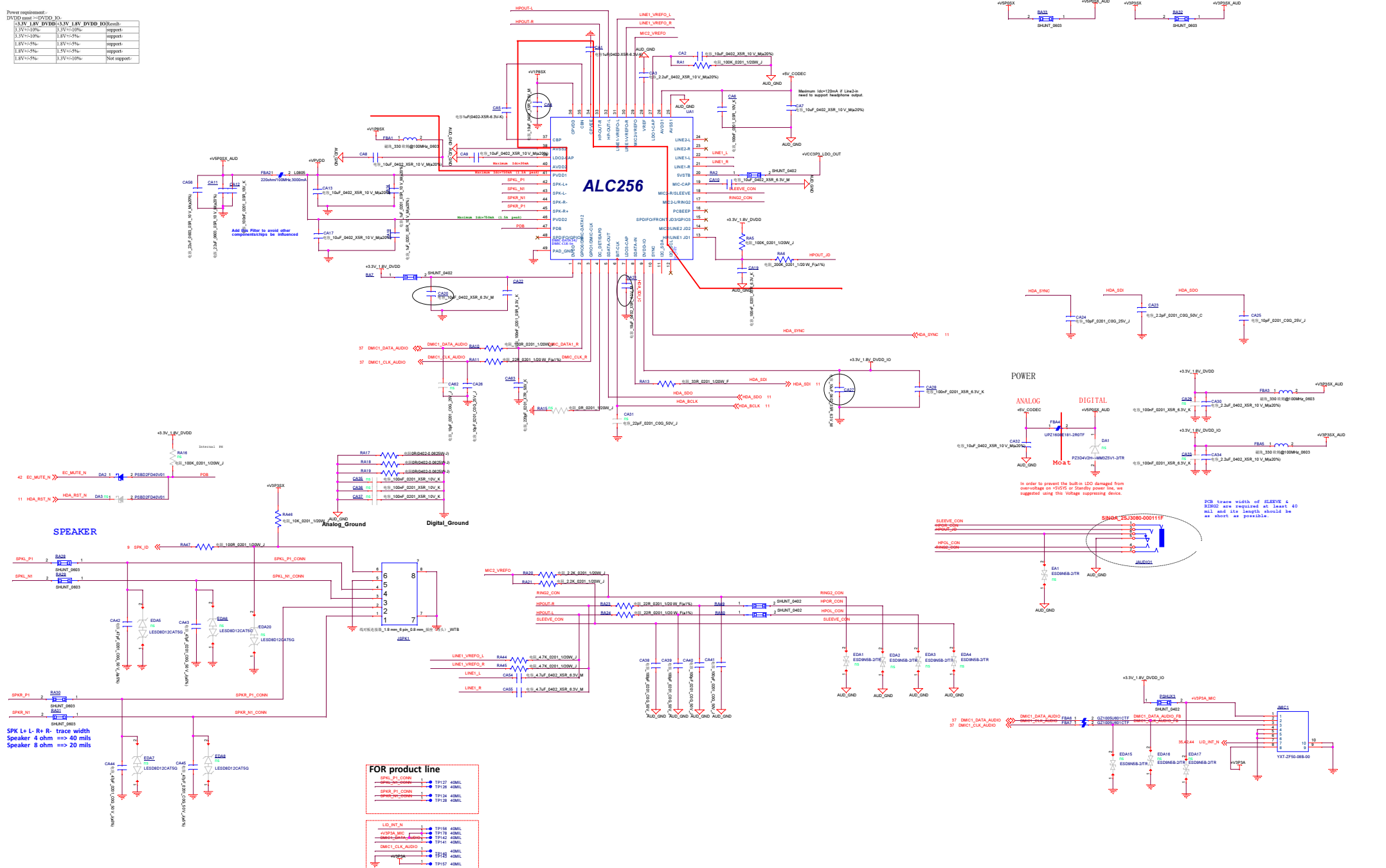
stuff CC short protection circuit - 12/26



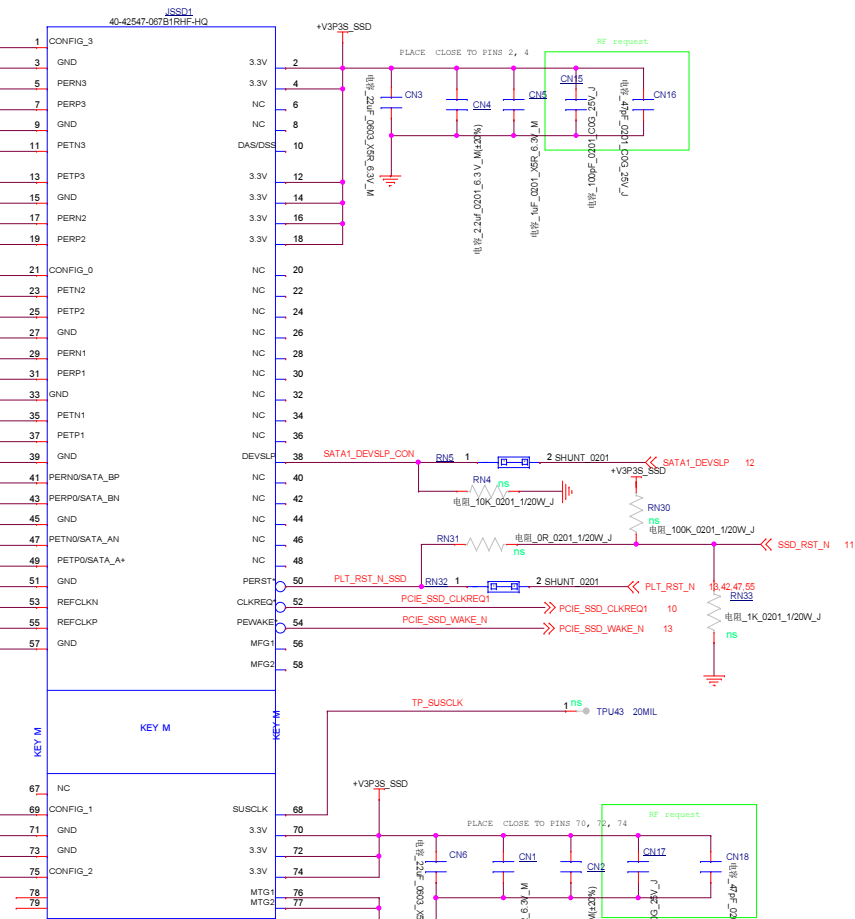
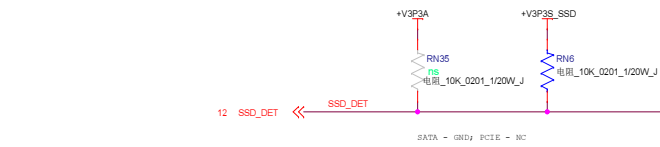
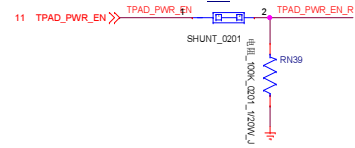
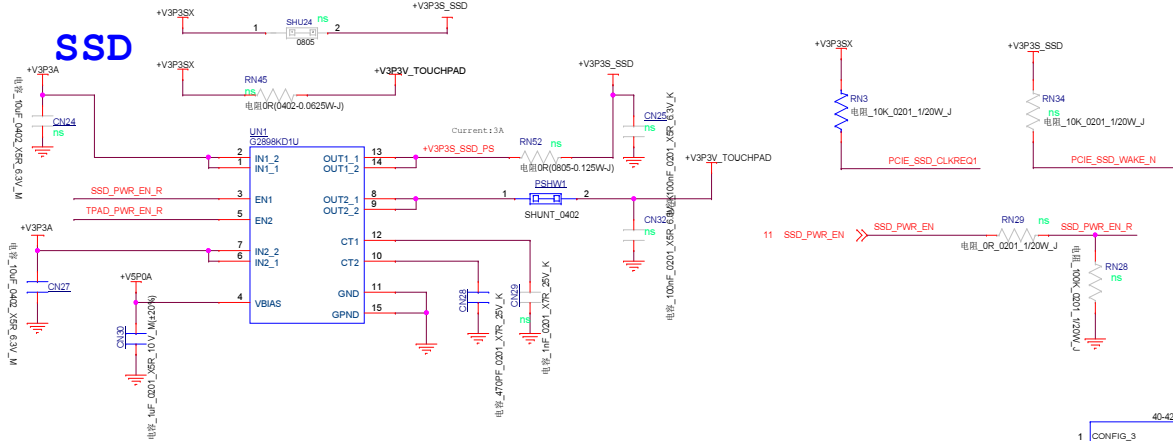


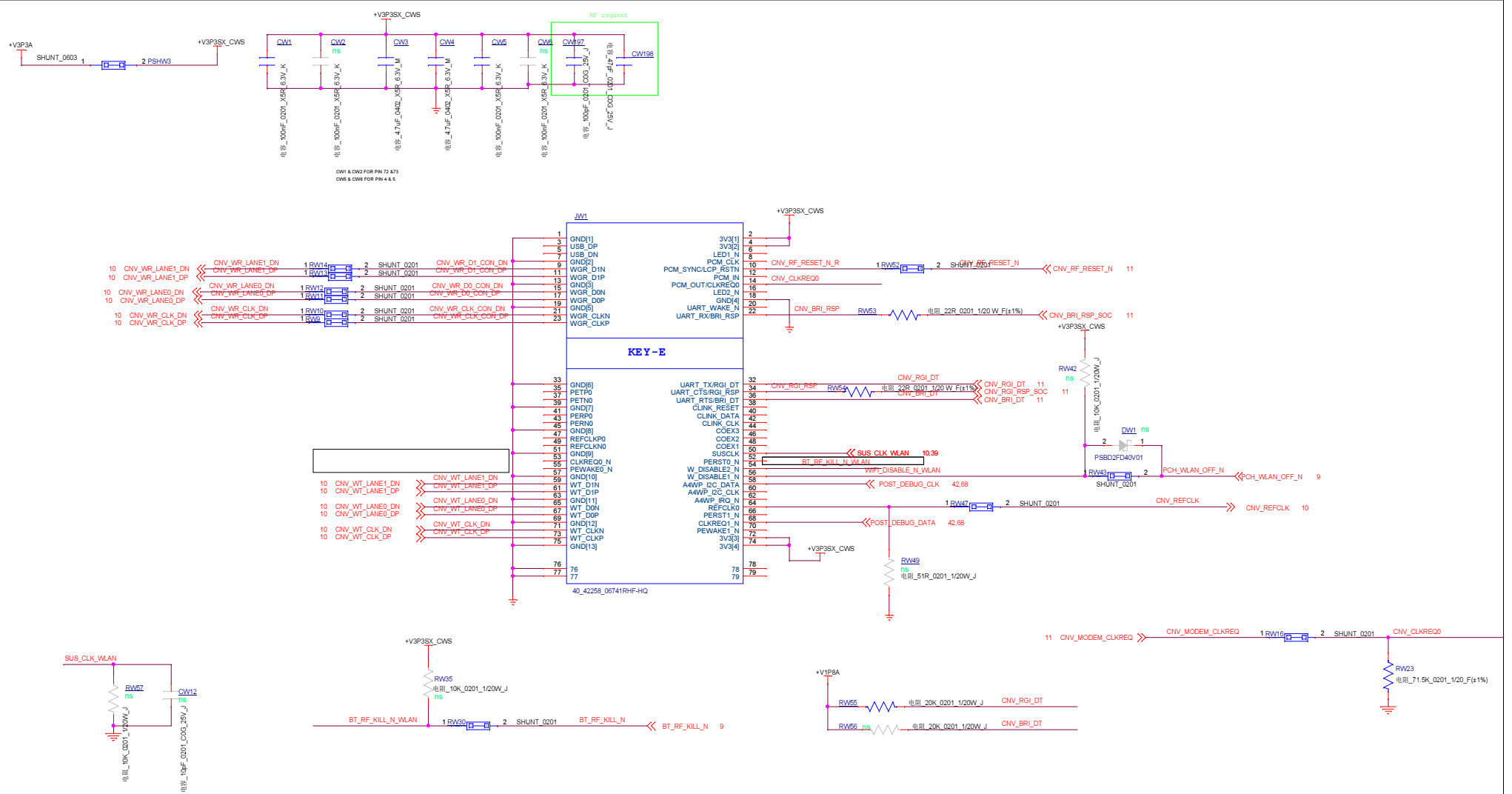


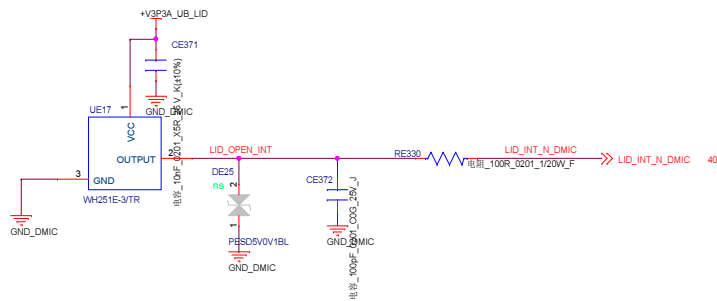
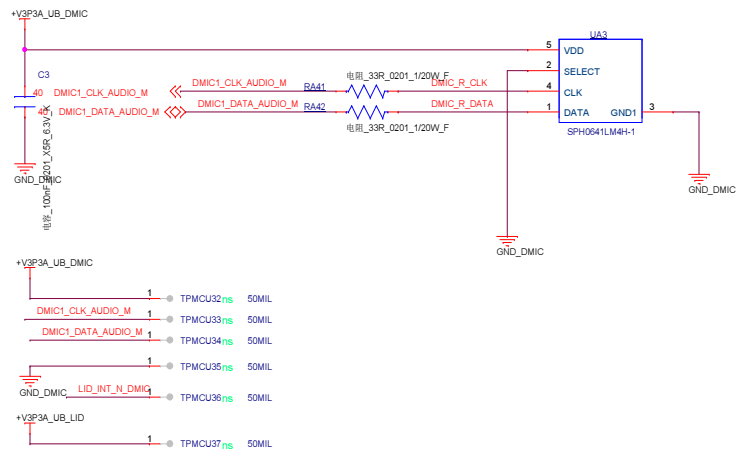
Power requirement:-			
DVDD must >= DVDD IO			
+3.3V 1.8V DVDD	+3.3V 1.8V DVDD IO	Result	
3.3V +/-10%	3.3V +/-10%	support	
3.3V +/-10%	1.8V +/-5%	support	
1.8V +/-5%	1.8V +/-5%	support	
1.8V +/-5%	1.5V +/-5%	support	
1.8V +/-5%	3.3V +/-10%	Not support	



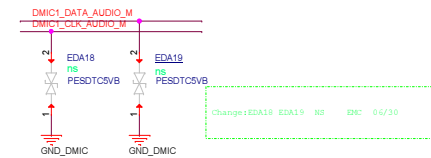
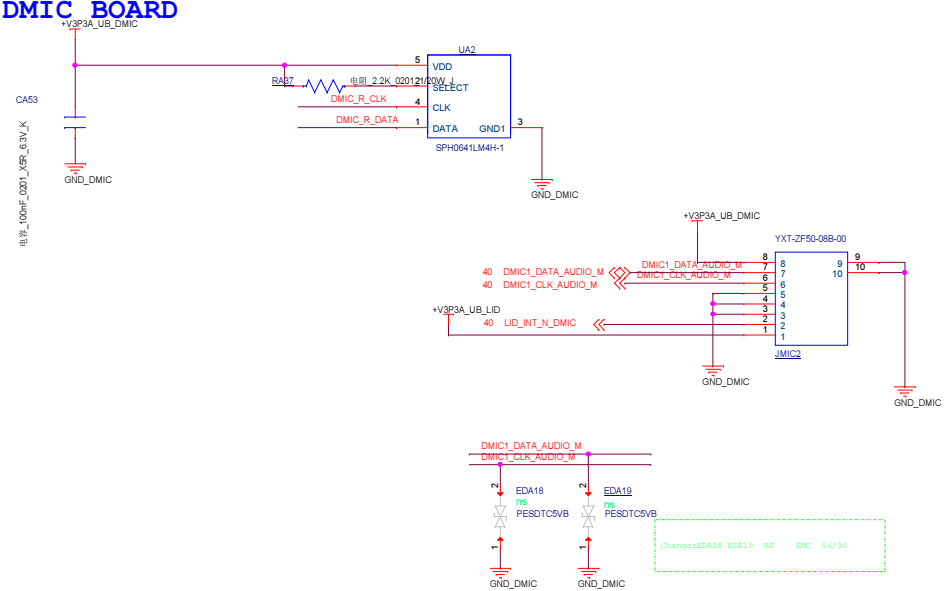
SSD



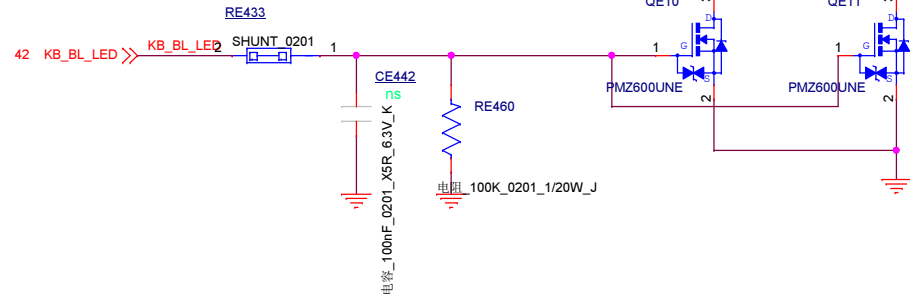
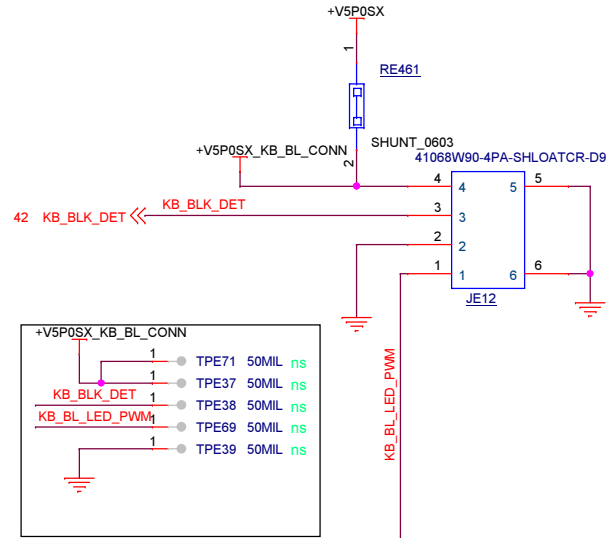
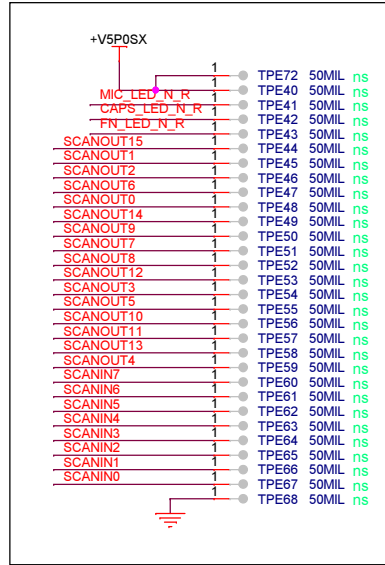




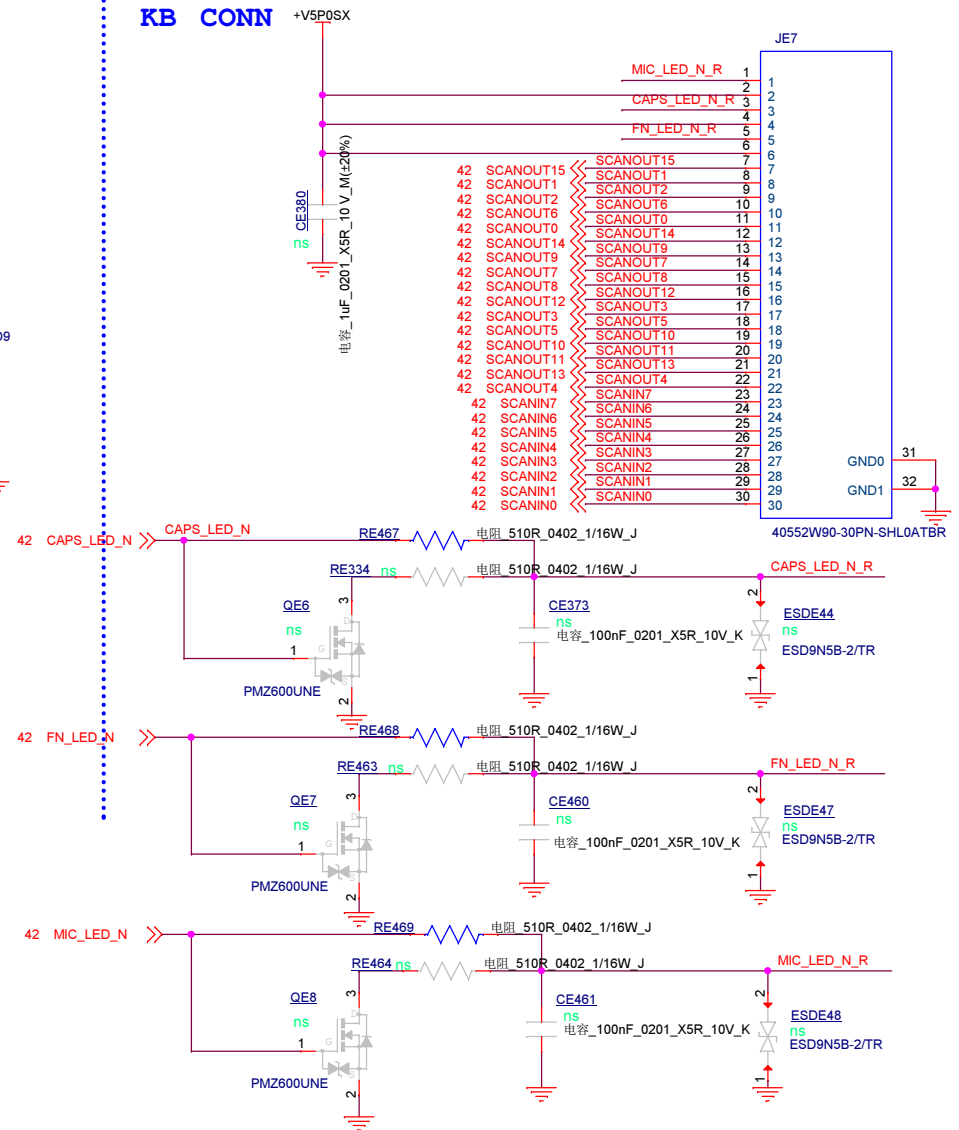
DMIC BOARD

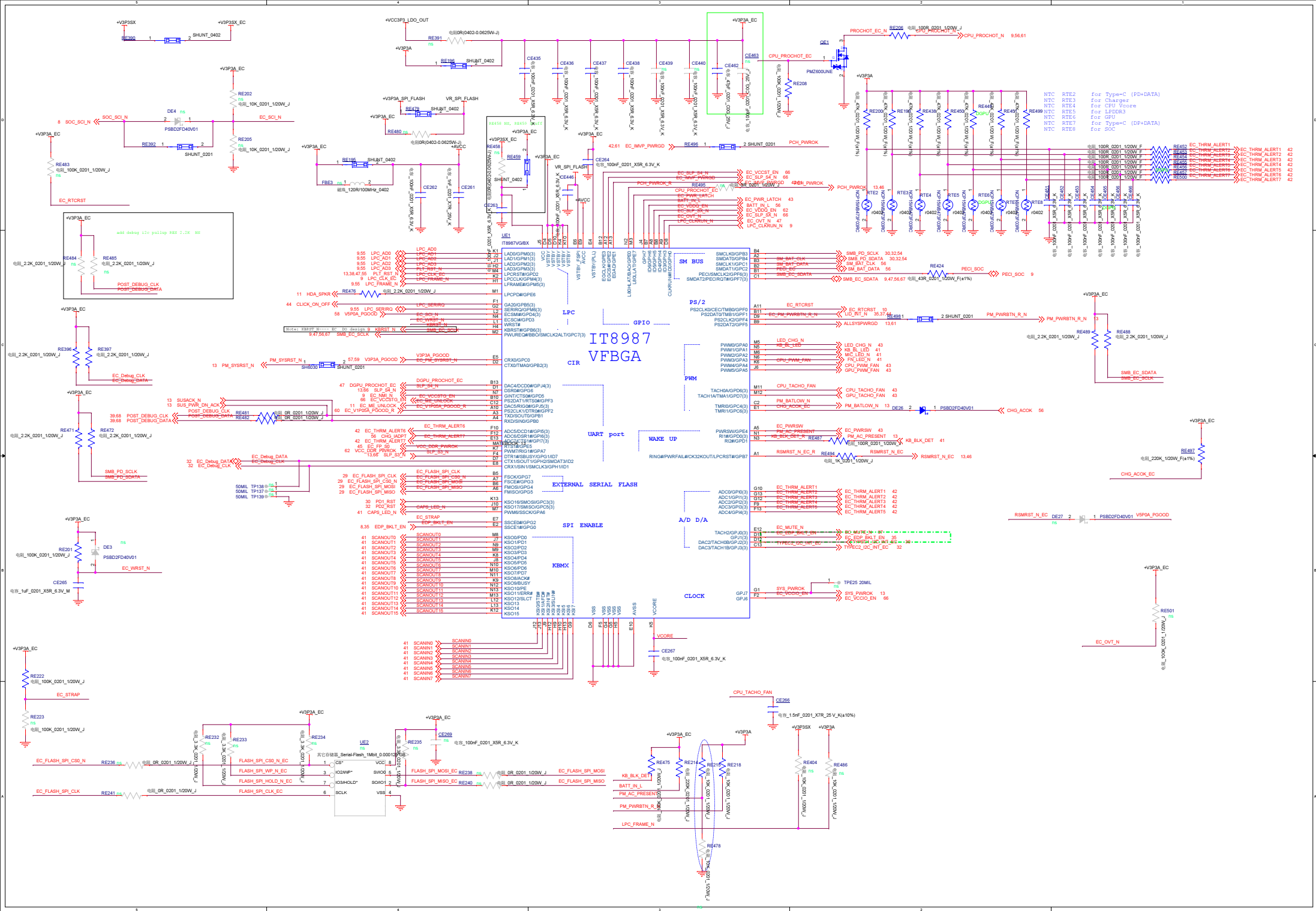


KB Backlight

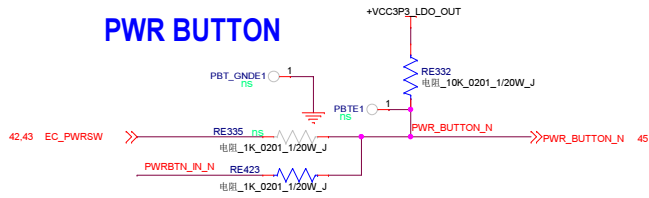


KB CONN

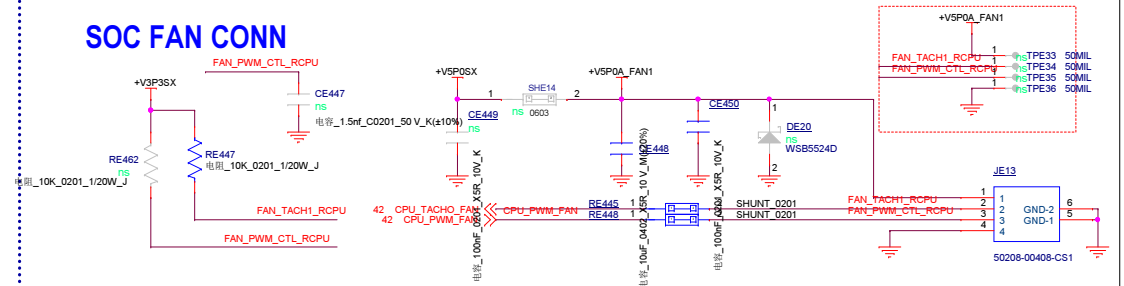




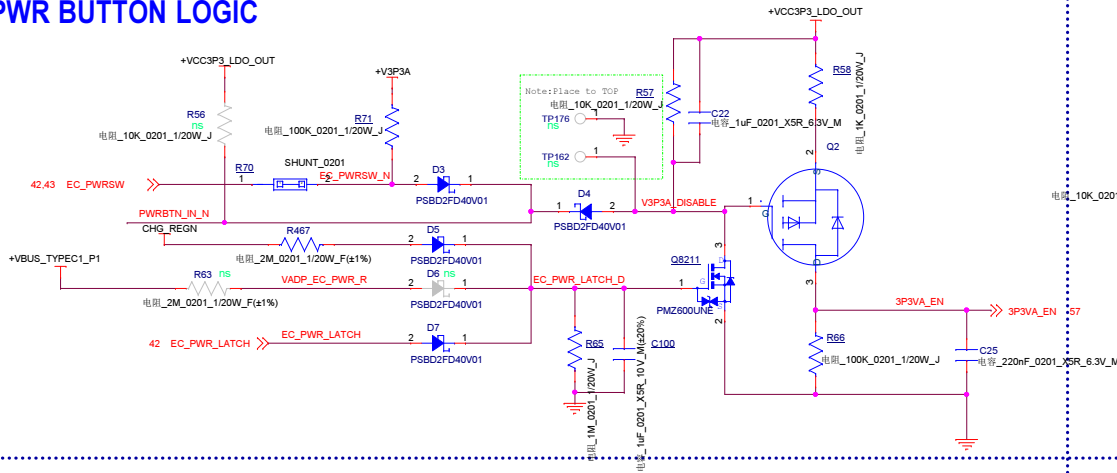
PWR BUTTON



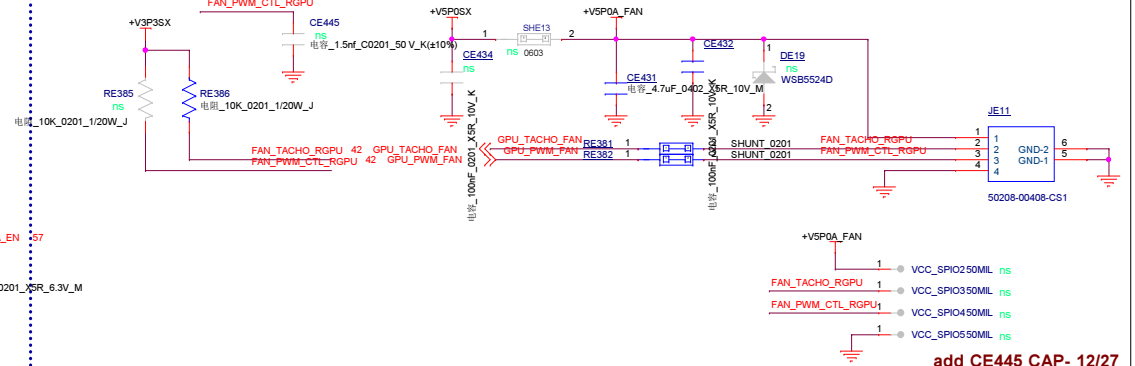
SOC FAN CONN



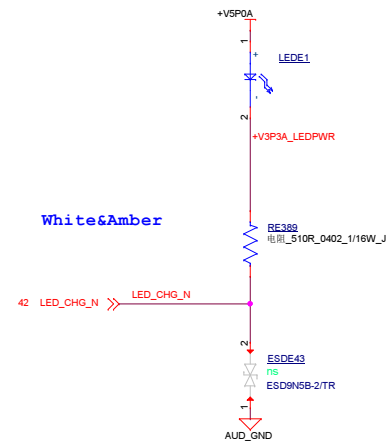
PWR BUTTON LOGIC



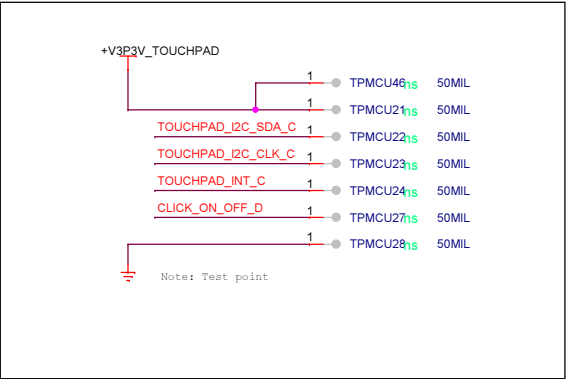
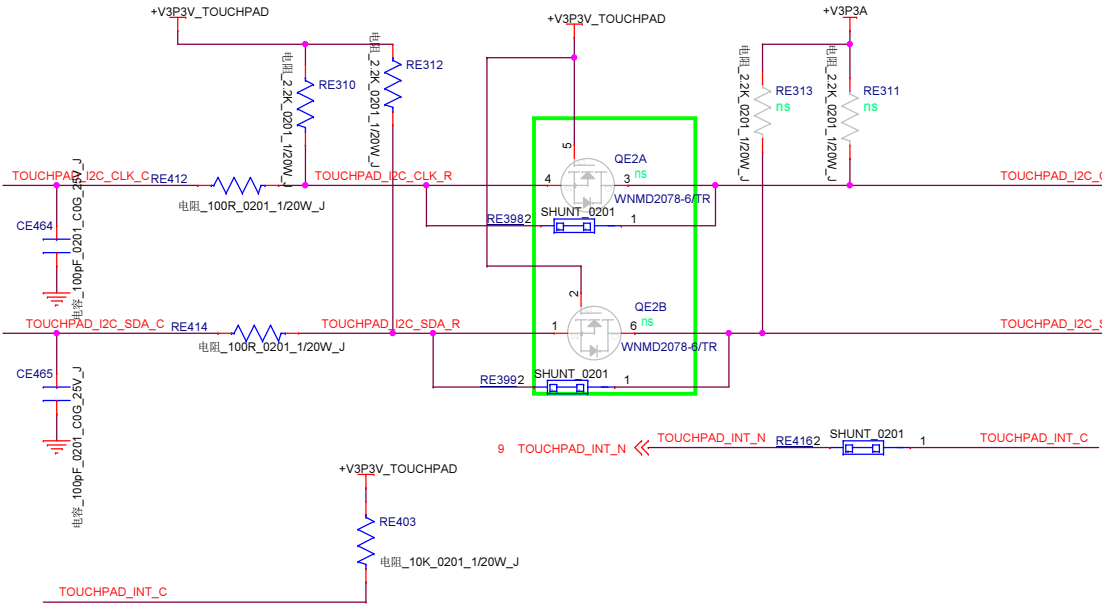
GPU FAN CONN



LED

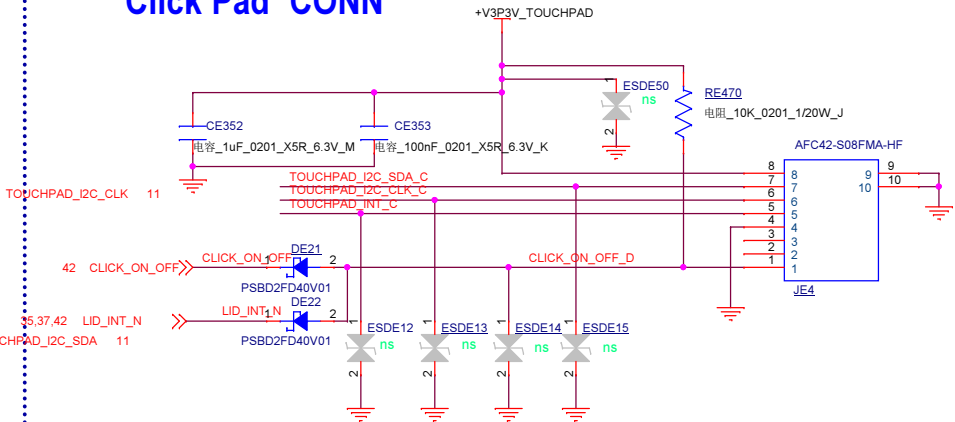


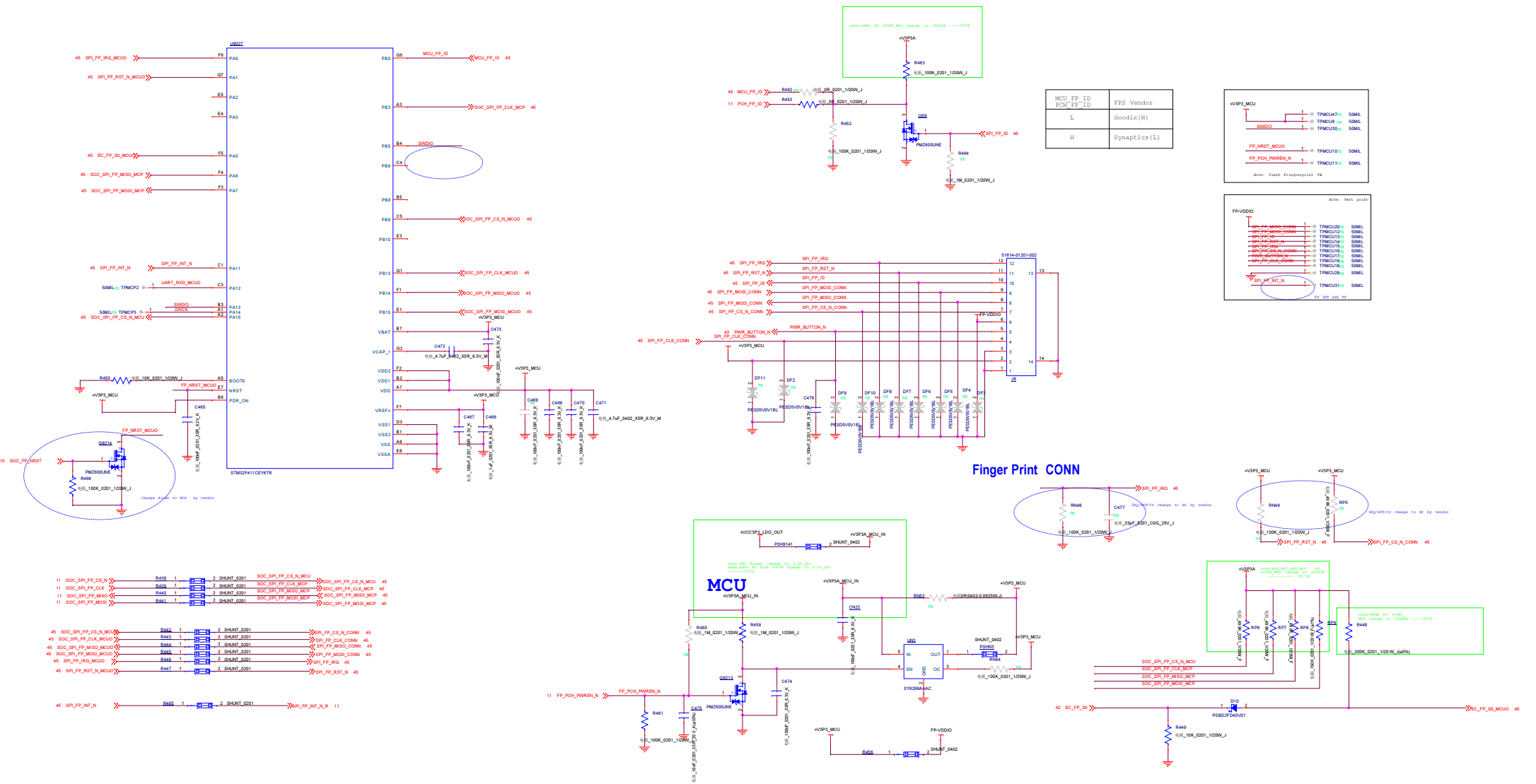
Touch Pad

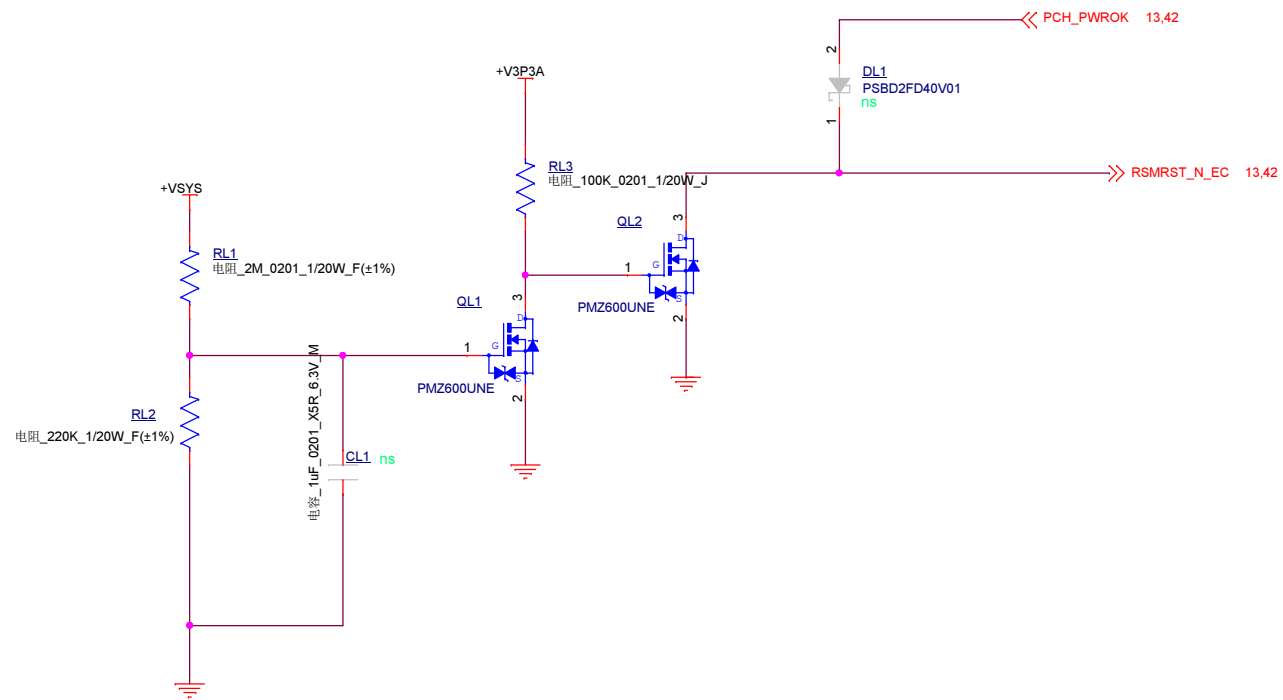


Click Pad CONN

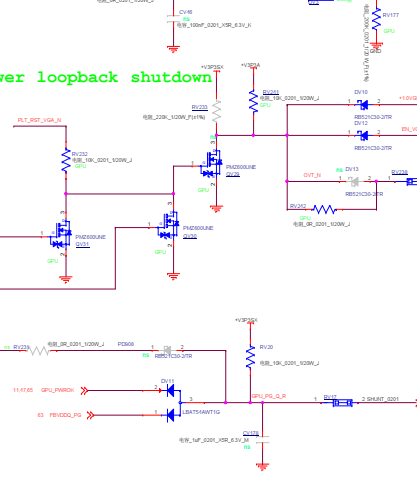
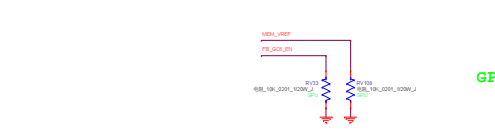
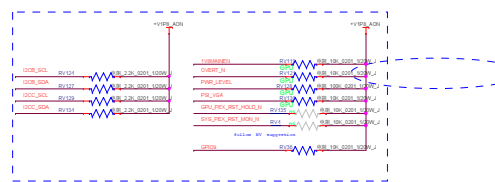
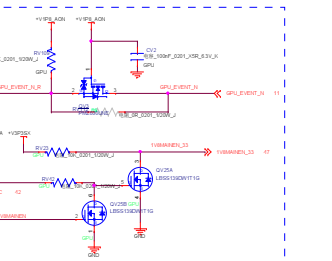
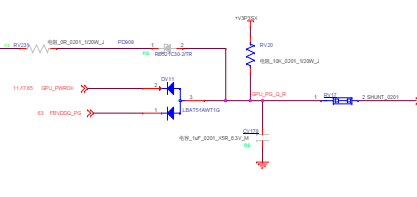
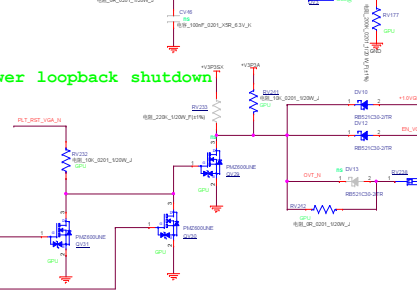
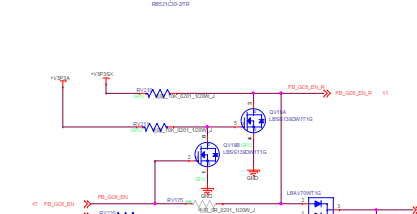
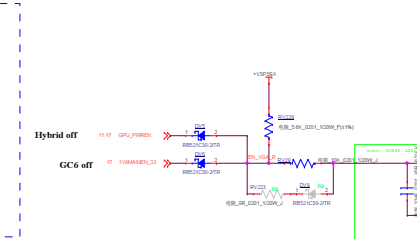
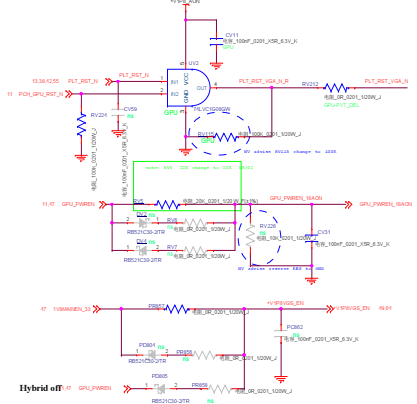
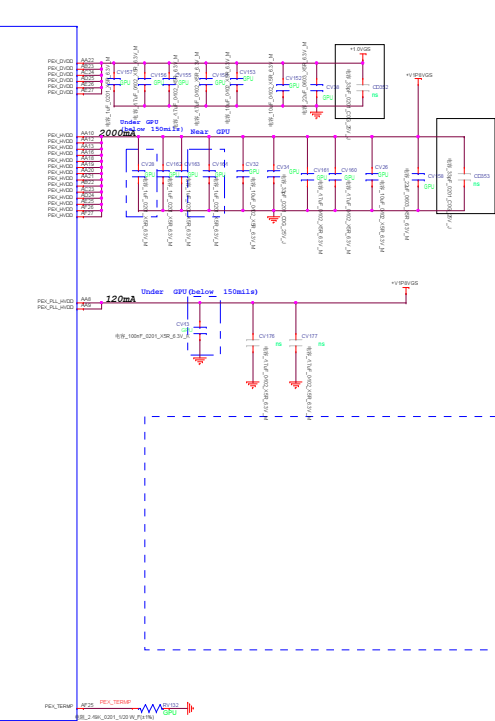
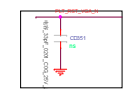
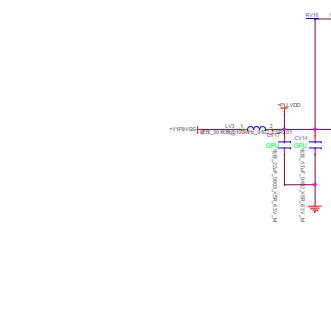
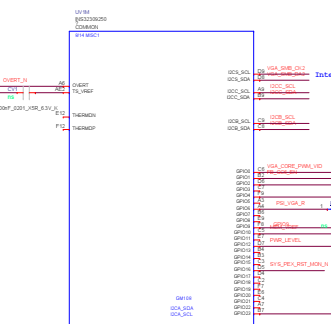
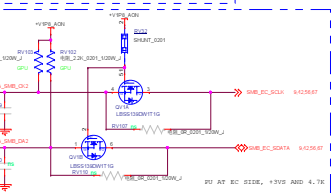
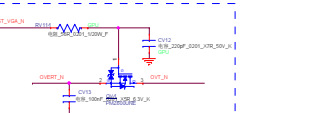
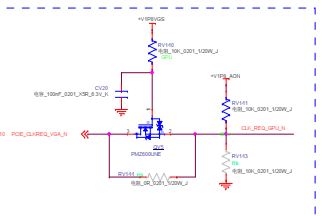
PIN1对 R n1

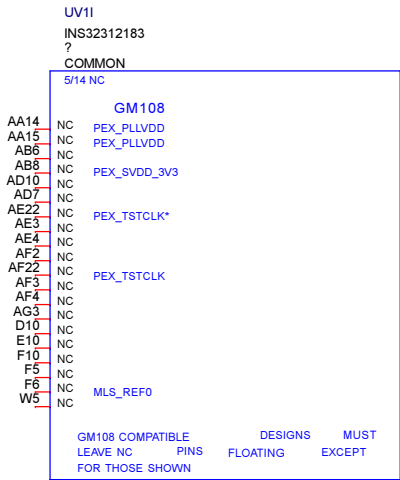
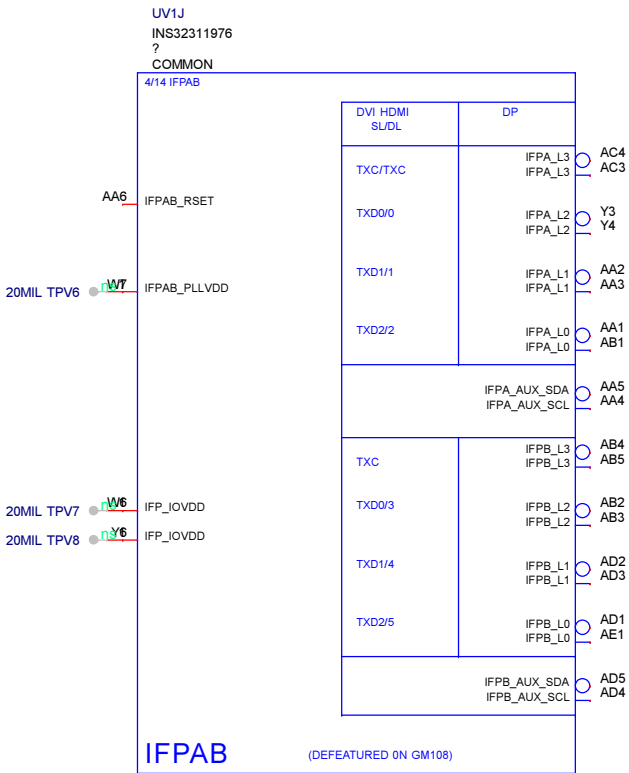
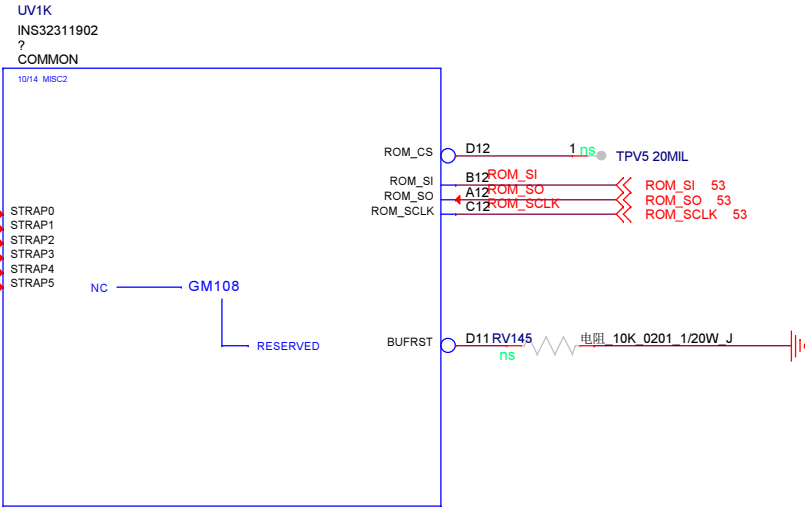
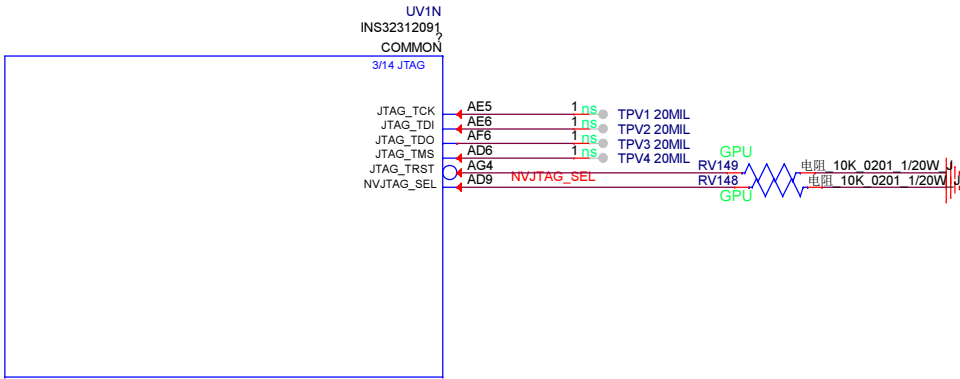






- 10 P0E_STN_CTL_NB-3
- 11 P0E_STN_CTL_P0-3
- 12 P0E_STN_CTL_P0-3
- 13 P0E_STN_CTL_P0-3





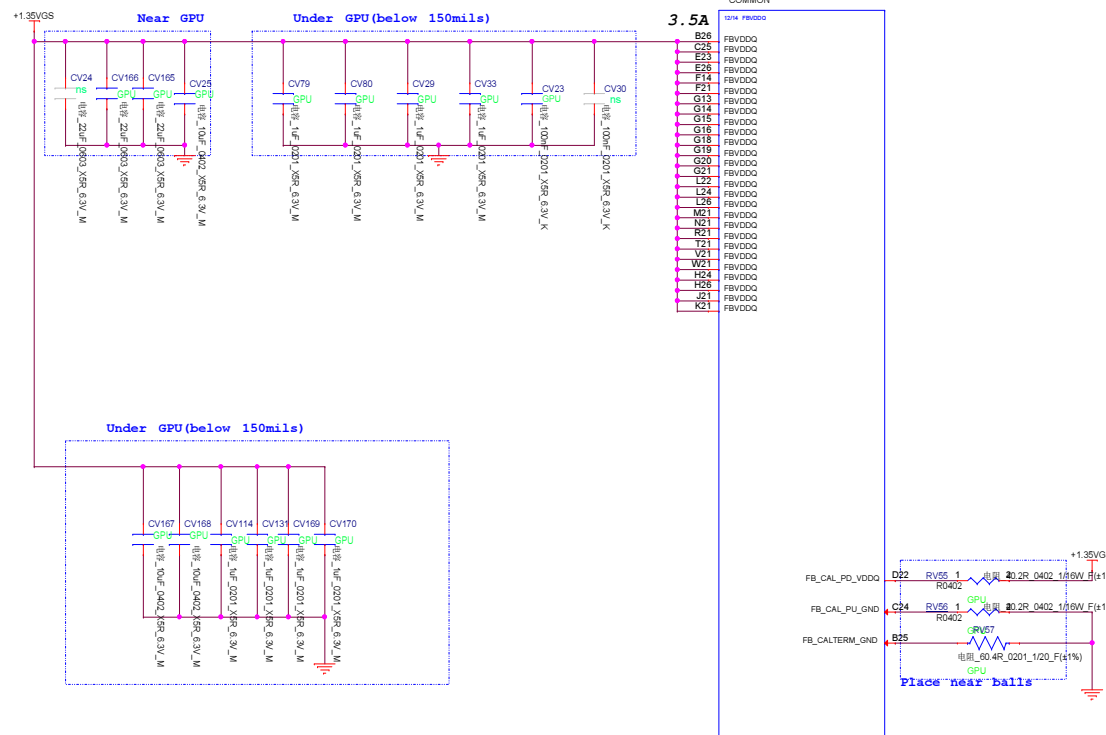
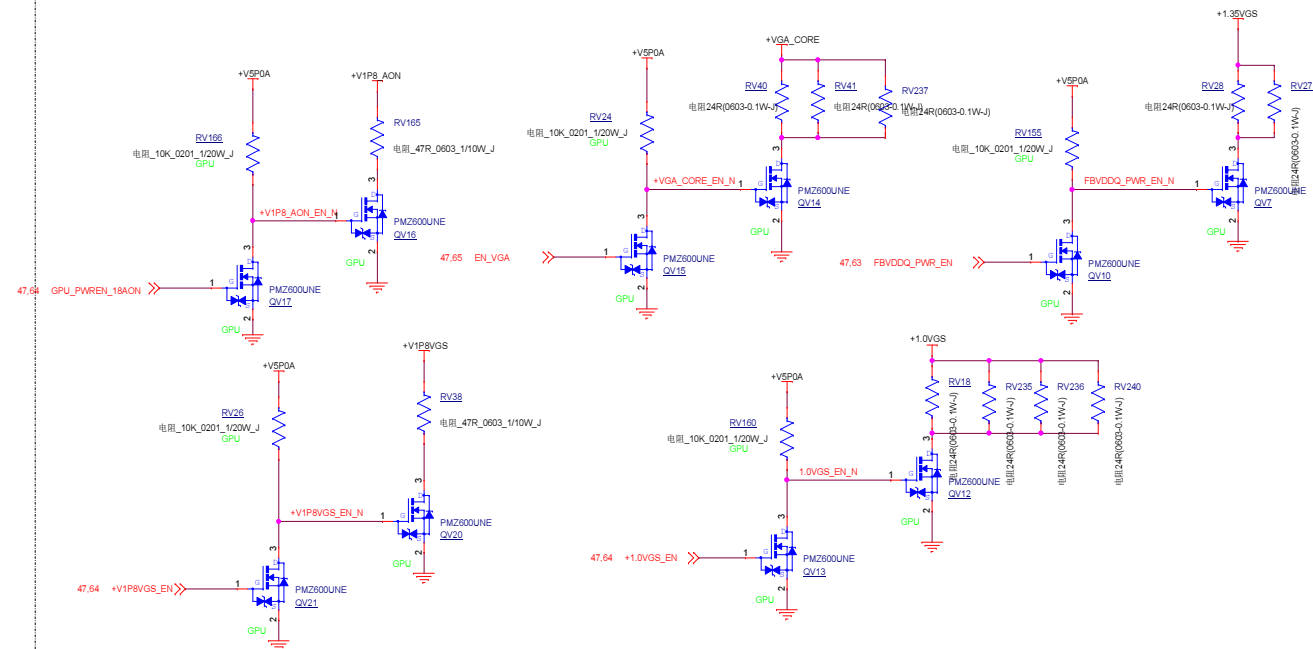
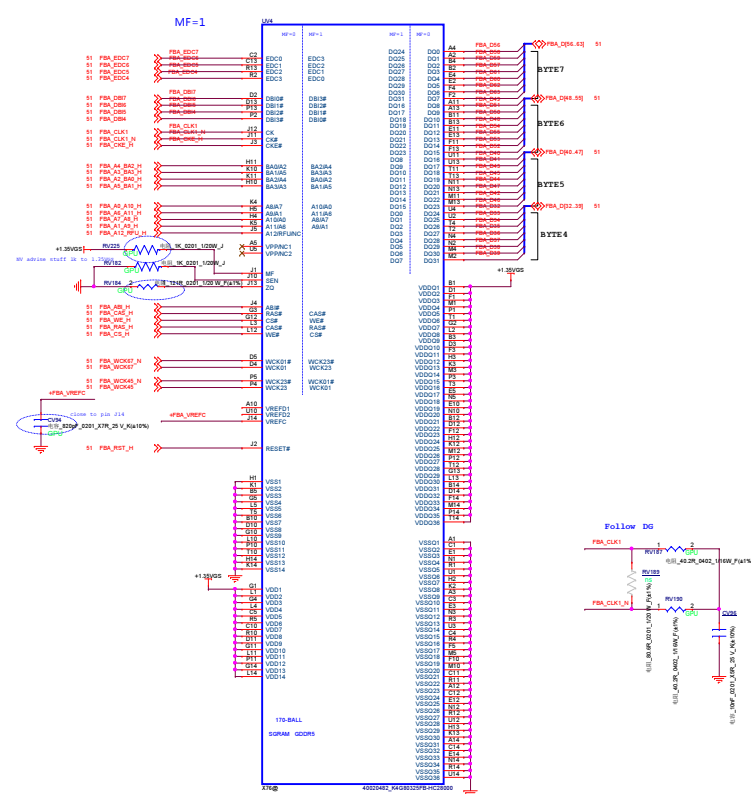


Table 9.18 GPU-Side FBVDDQ Decoupling Requirements

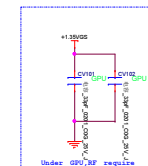
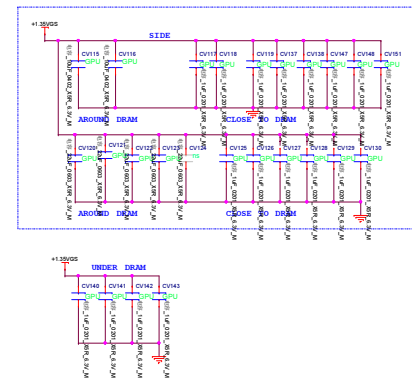
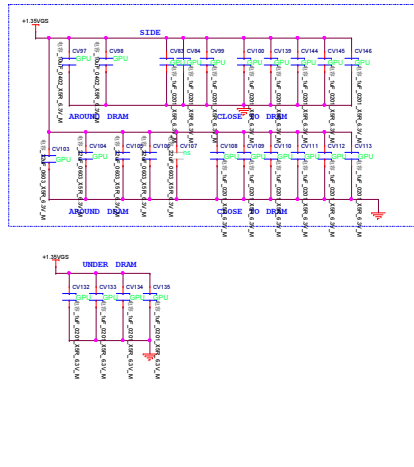
Decoupling Capacitor		Recommended Quantity and Placement (for all supported partitions combined)	
Capacitance	Type Size	Quantity	Placement
For N17x GPU Package: GB2C-64 (preliminary)			
1.0 uF	X6S [0402]	8	Under GPU FBVDDQ ball (evenly distributed throughout partition)
10 uF	X6S [0603]	2	
10 uF	X6S [0603]	1	Near GPU device
22 uF	X6S [0603]	3	
For N17x GPU Package: GB4C-128 (preliminary)			
1.0 uF	X6S [0402]	12	Under GPU FBVDDQ ball (equally distributed across partitions)
10 uF	X6S [0603]	4	
10 uF	X6S [0603]	2	Near GPU device
22 uF	X6S [0603]	5	
For N17x GPU Package: GB4-256			
1.0 uF	X6S [0402]	24	Under GPU FBVDDQ ball (equally distributed across partitions)
10 uF	X6S [0603]	5	
10 uF	X6S [0603]	7	Near GPU device
22 uF	X6S [0603]	9	



Memory - Upper 32 bits



Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type [Size]	Quantity	Placement (by DRAM Interface Mode)
Combined FBVDD-FBVDVQ Rail			
1.0 uF	X65 [4003]	10	For x32 DRAM: Under the DRAM FBVDD or FBVDVQ ball.
10 uF	X65 [0603]	4	For x16 DRAM in a "clamshell" PCB configuration: as close to DRAM periphery as possible. Ensure at least 2 GND vias and 2 power vias for each decoupling capacitor.
1.0 uF	X65 [4002]	8 additional	For x32 DRAM: Choose x32 interface to achieve the maximum DRAM speeds. Add these additional decoupling caps under the DRAM FBVDD/Q ball; should spare existing FBVDD/Q ball via if possible. See Figure 9.23 for an example.
10 uF	X65 [0603]	2	Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.
22 uF	X65 [0603]	5	Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor. For a 4-GHz WCK (8 Gbps data rates): Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.

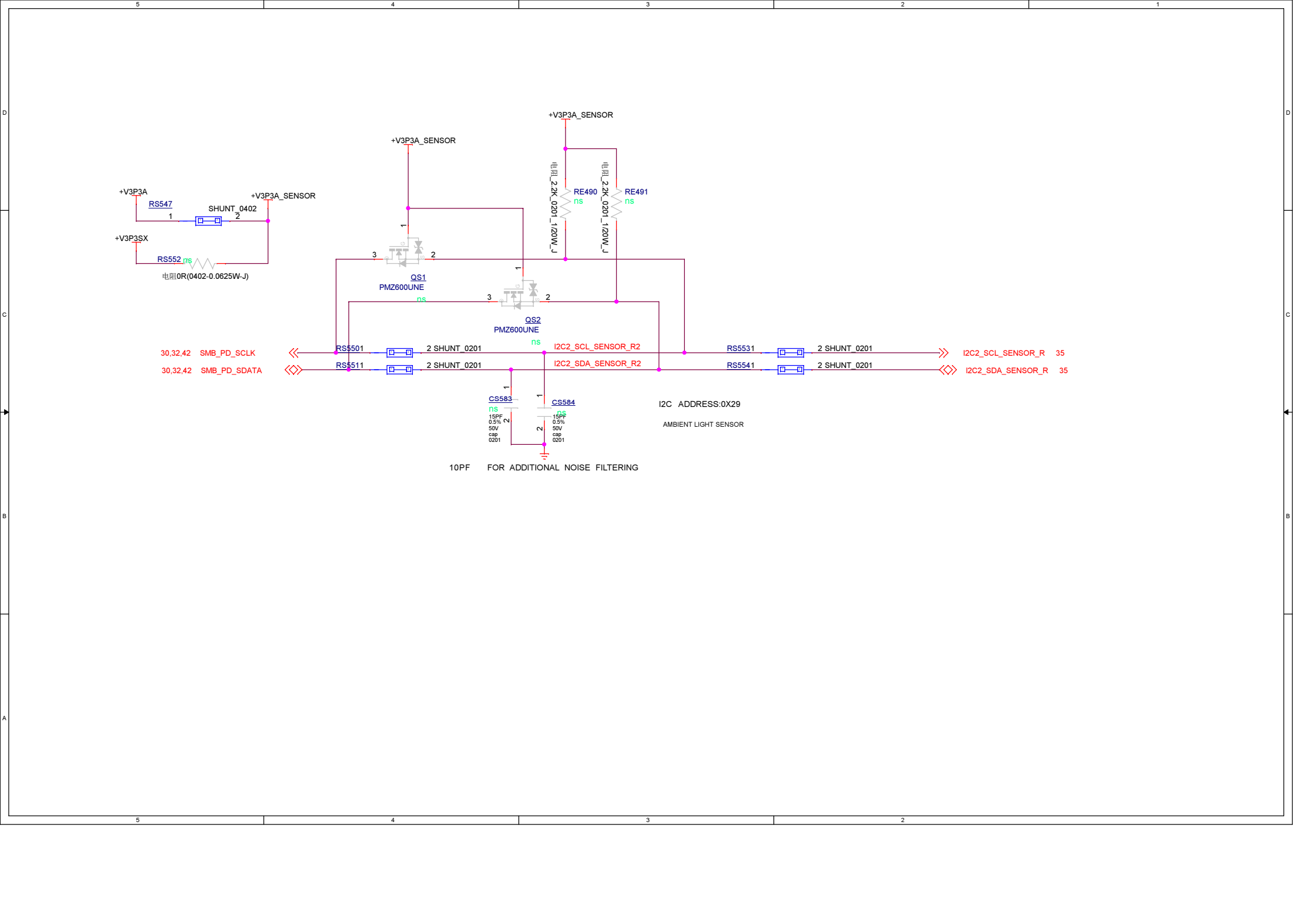


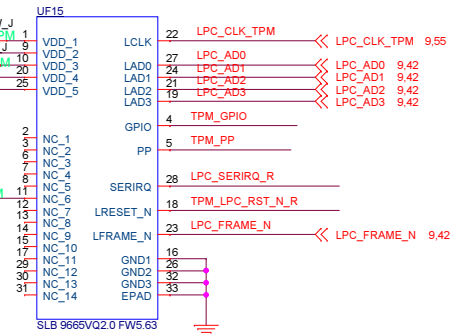
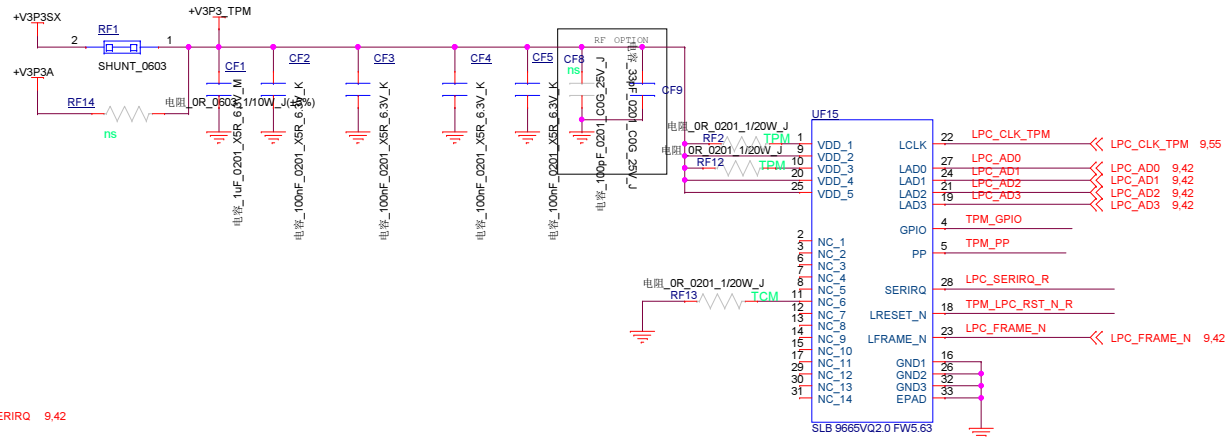
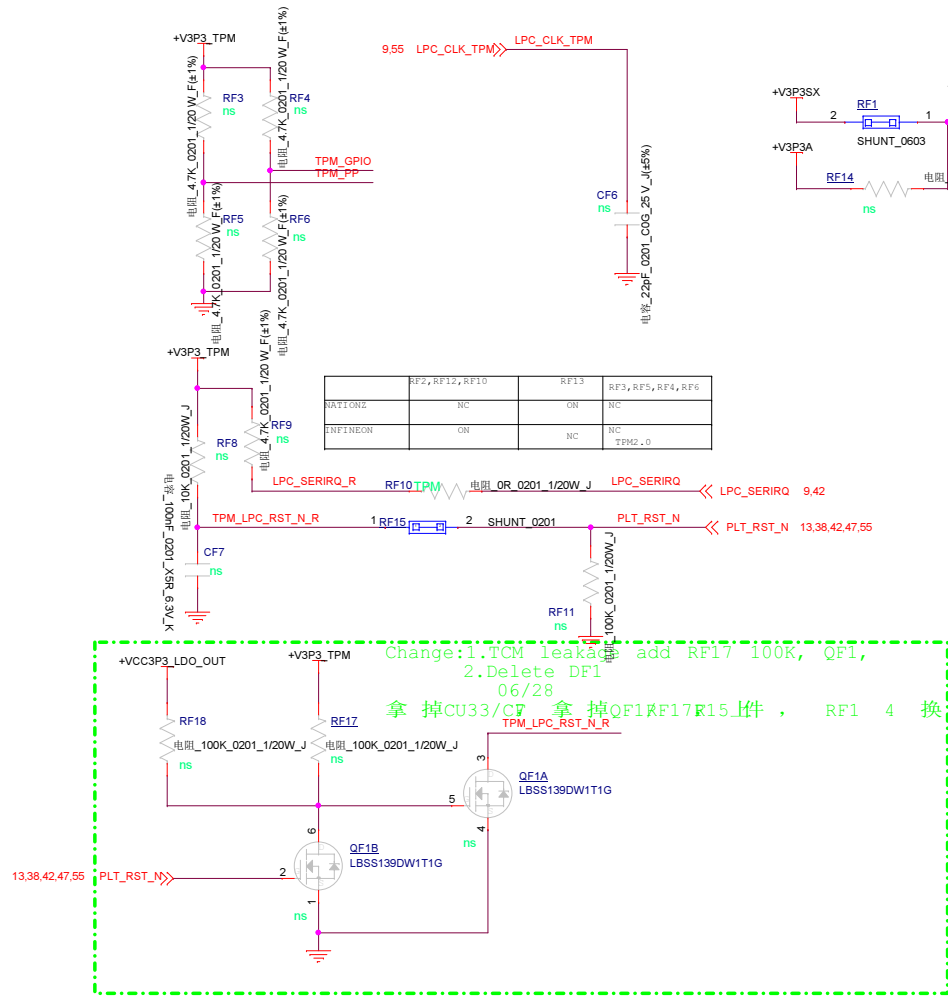


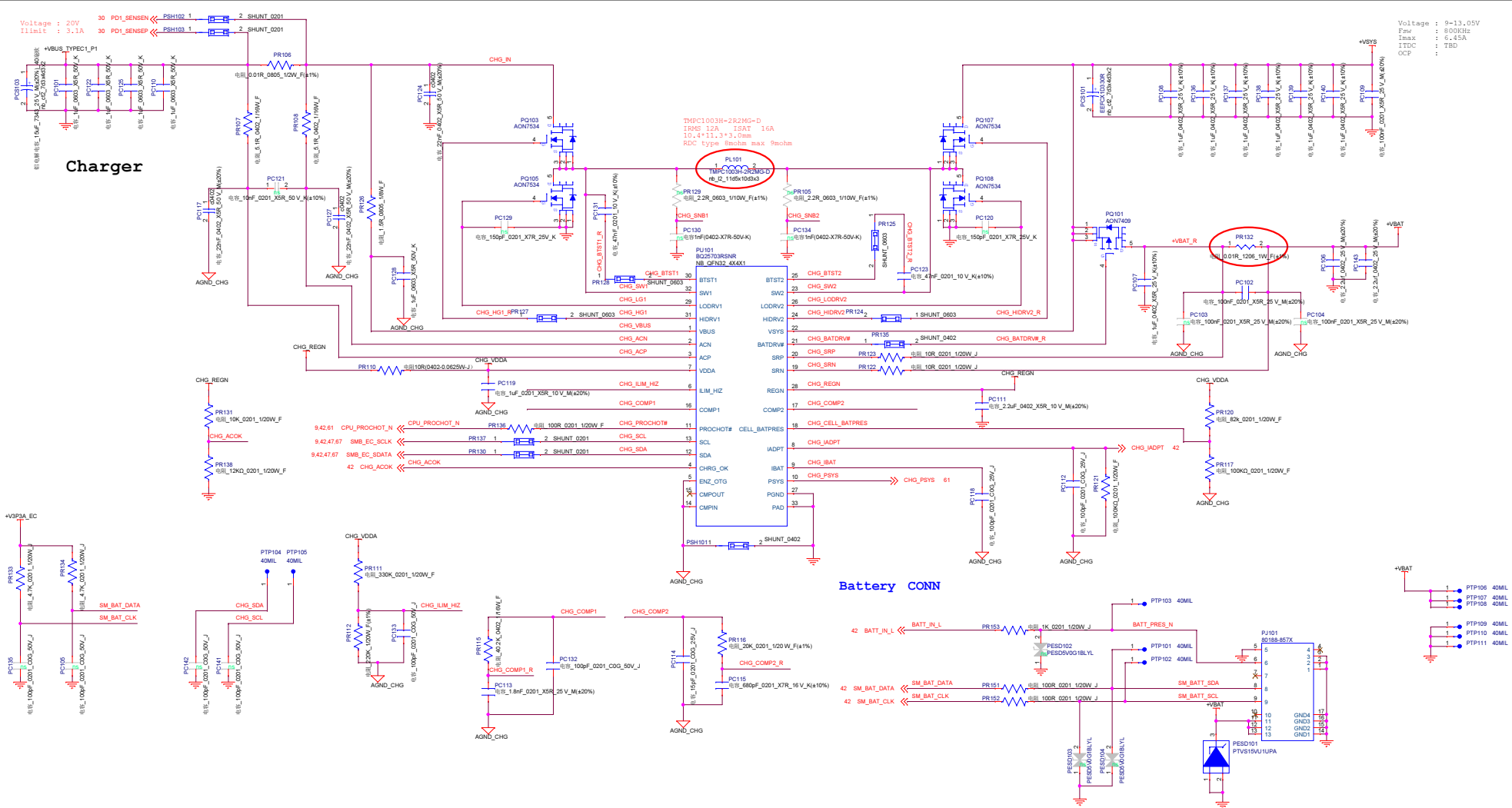
Physical Strapping pin	Power Rail	RAM_CFG[3]	RAM_CFG[0x02]	RAM_CFG[0x01]	RAM_CFG[0x00]
STRAP0			L	H	L
STRAP1			H	L	L
STRAP2			L	L	L

VGA DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

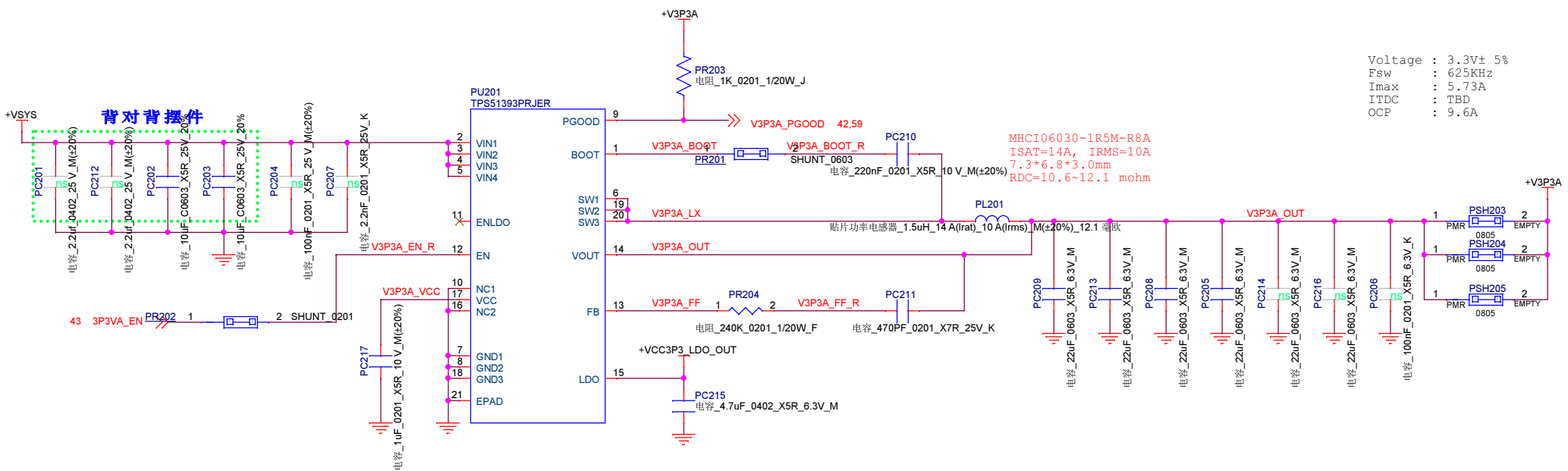
Physical Strapping pin	Power Rail	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SCLK	M	Disable	Disable	Disable	Disable
ROM_SI	H				
ROM_SO	H				

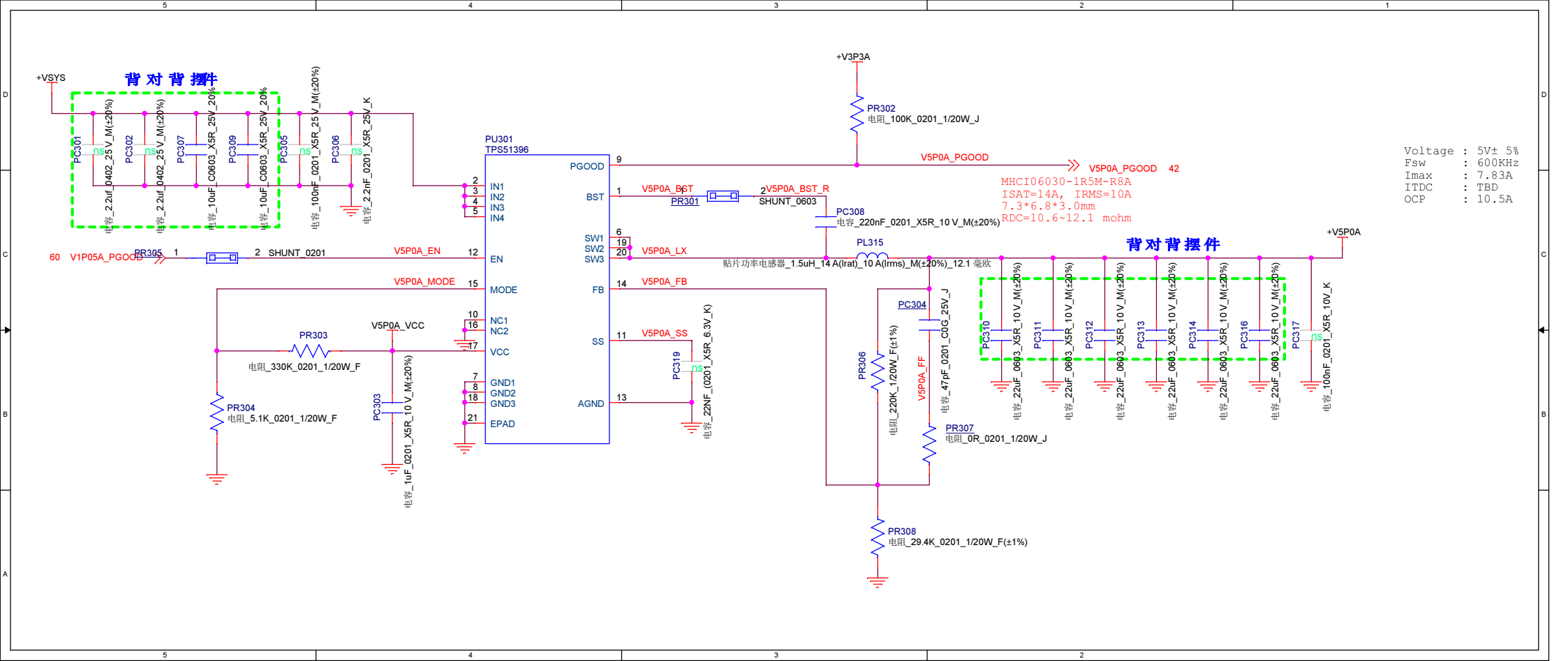


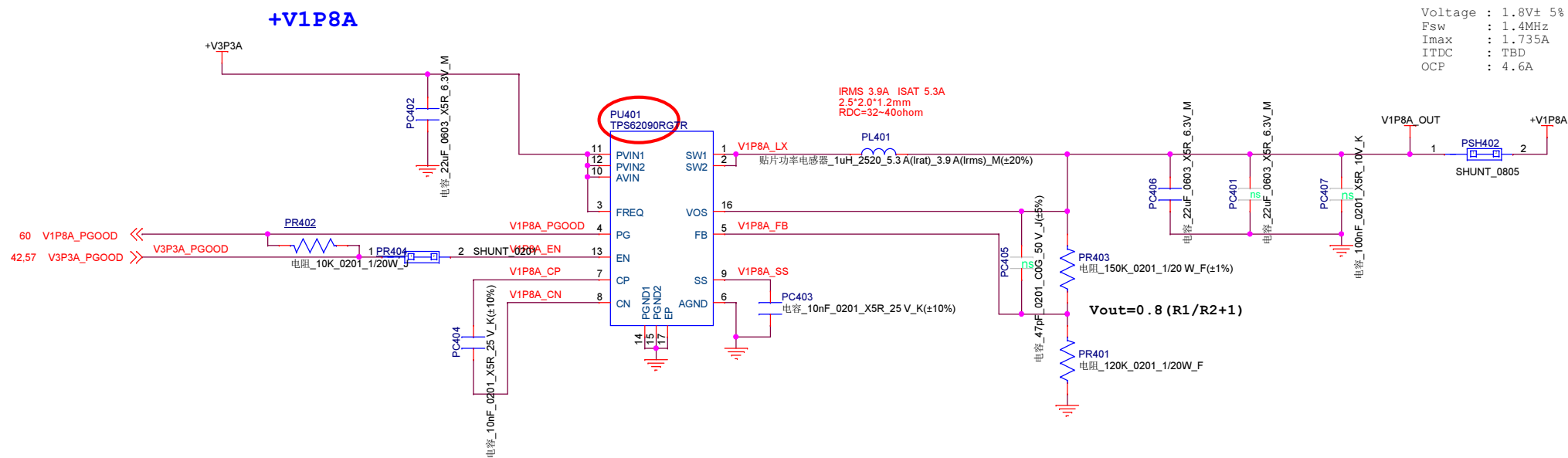




+V3P3A



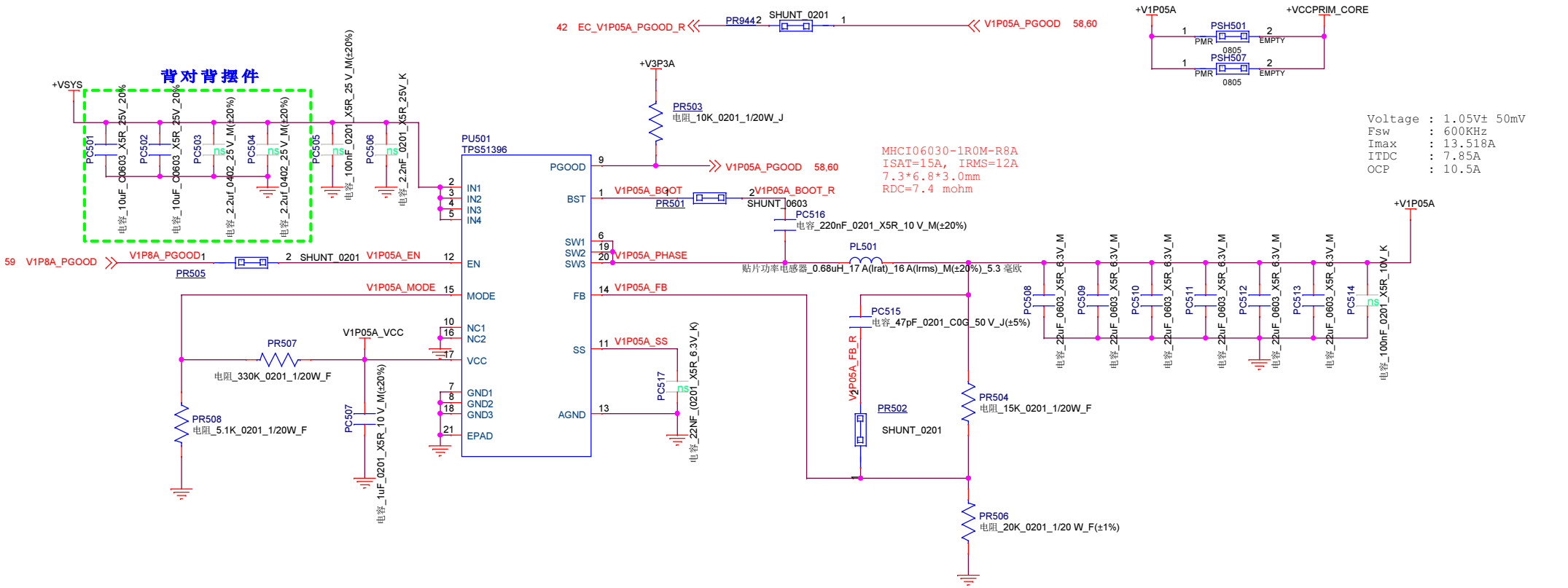


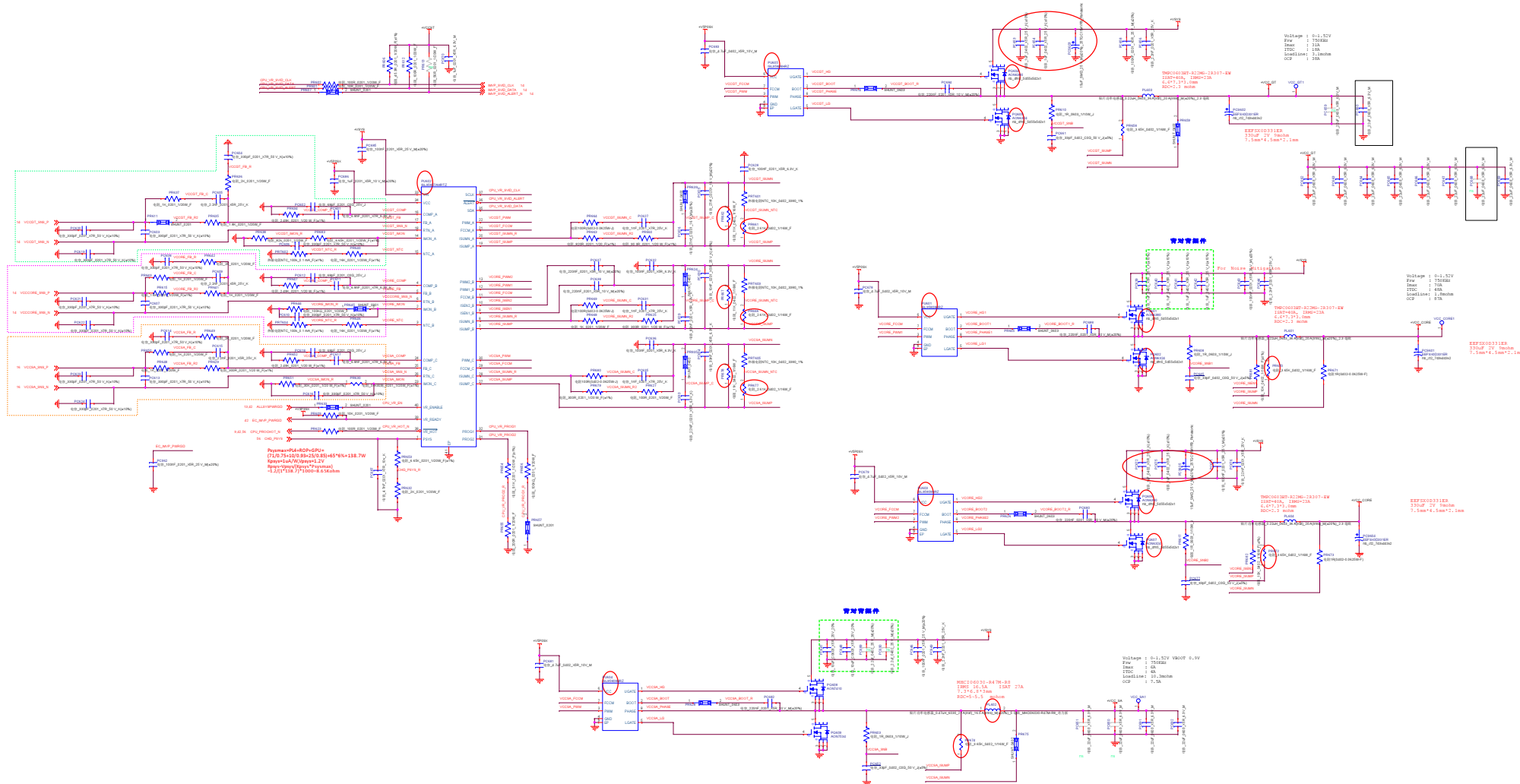


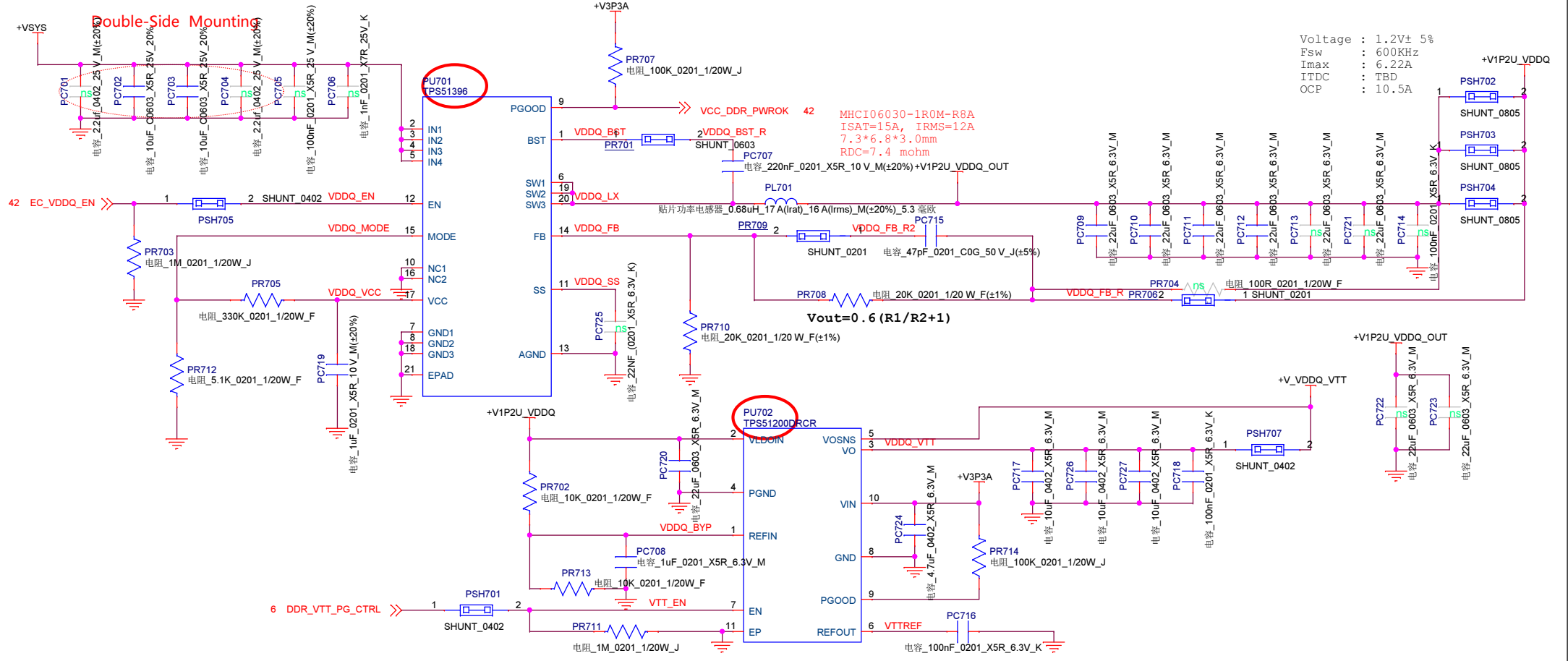
Voltage : 1.8V± 5%
Fsw : 1.4MHz
Imax : 1.735A
ITDC : TBD
OCP : 4.6A

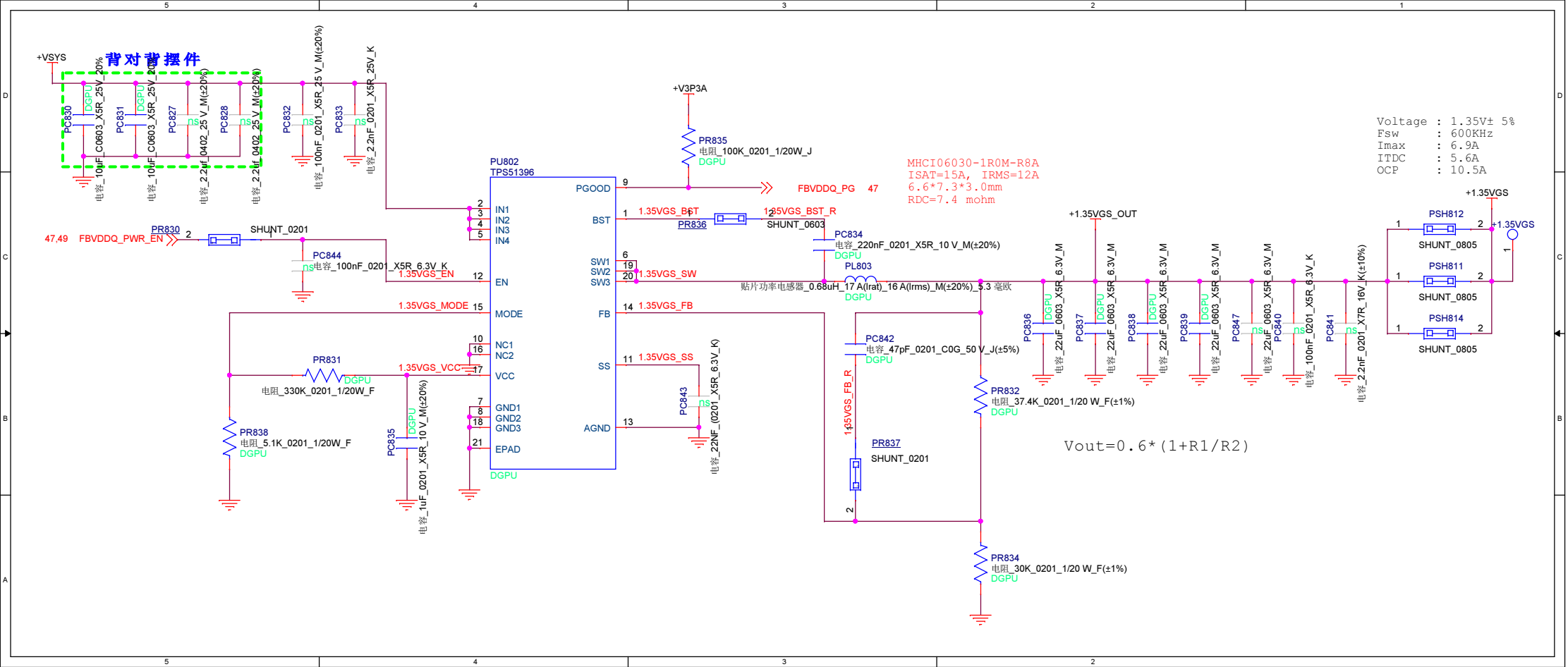
+V1P05A

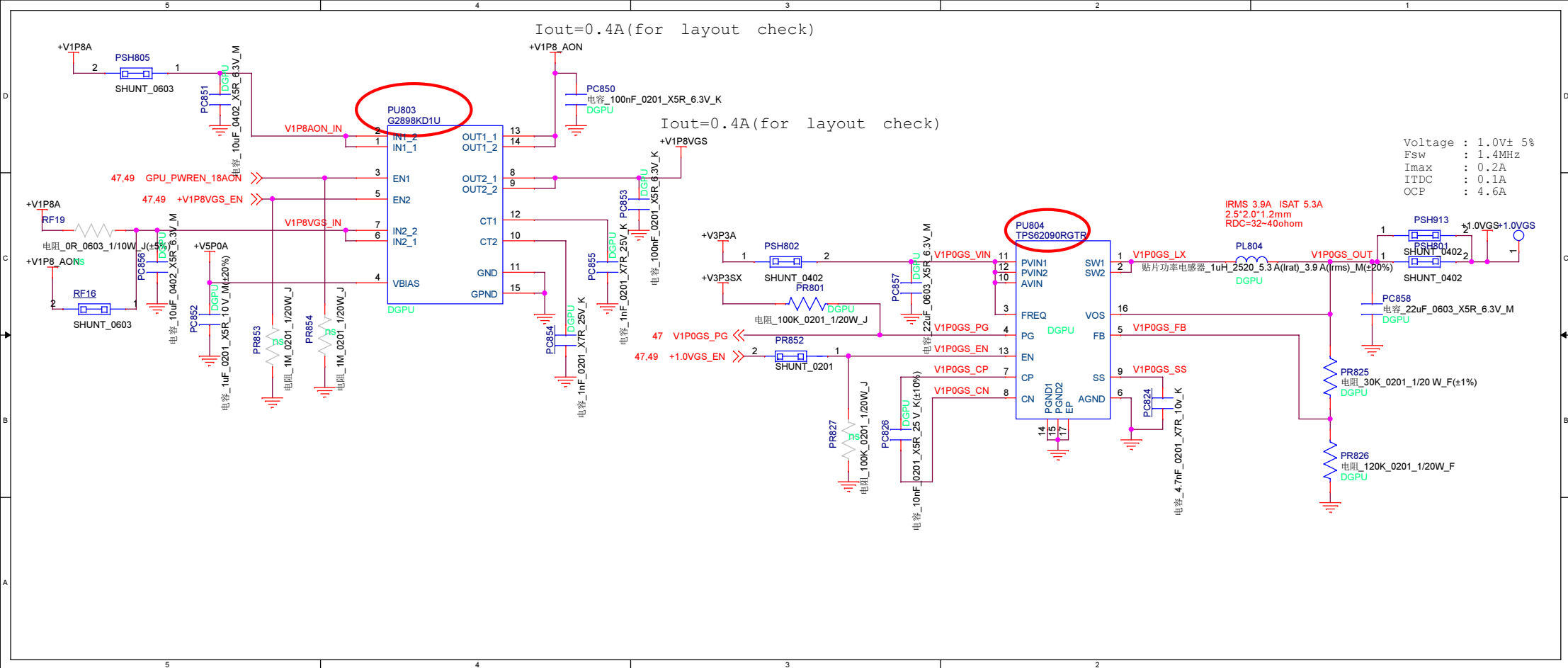
背对背摆件

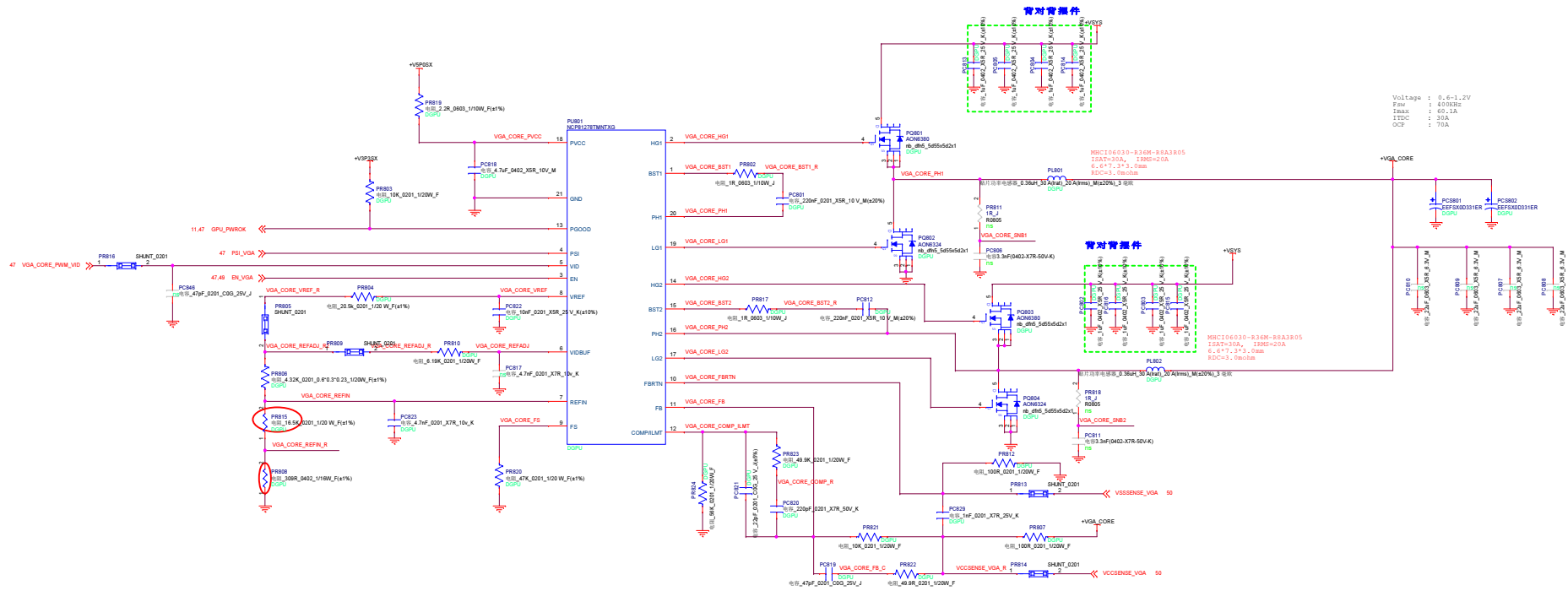






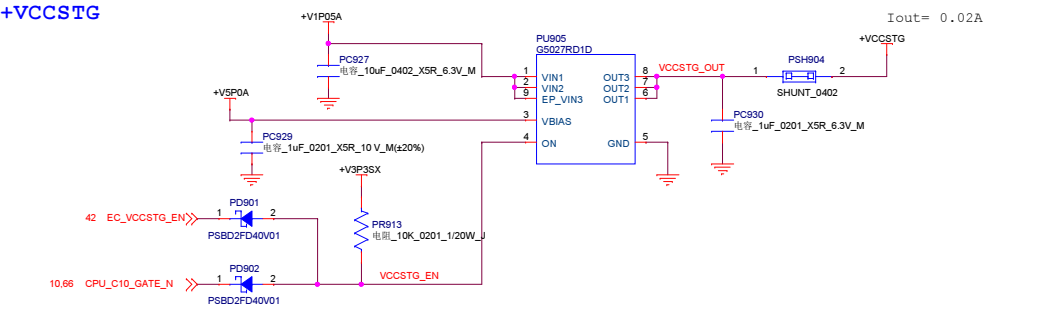






Voltage : 0.6-1.2V
Fsw : 400KHz
Imax : 60.1A
ITDC : 30A
OCF : 70A

+VCCSTG



+V1P2U_VCCSFR_OC

